Description

XN406 is a high-performance broadband fractional-N frequency synthesizer. It integrates the reference buffer, reference divider, PFD/CP, voltage controlled oscillator (VCO), RF divider, automatic frequency control (AFC) unit, Delta-Sigma modulator, phase-locked detection and other units, and supports SPI bus control. The RF output frequency can be up to 3000MHz and down to 25MHz. Package type: QFN40L (0606×0.75-0.50).

Features

- Integrated broadband VCO
- Low phase noise
- High phase detector frequency

Device Features

Designation	Package Type	Package Size	Operating Temperature
XN406	QFN40L	6mm×6mm×0.75mm	-40℃～105℃

Typical Applications

- Base stations for Mobile Radio
- WLAN and WiMAX

Functional Diagram

The functional diagram is shown in Figure 1.

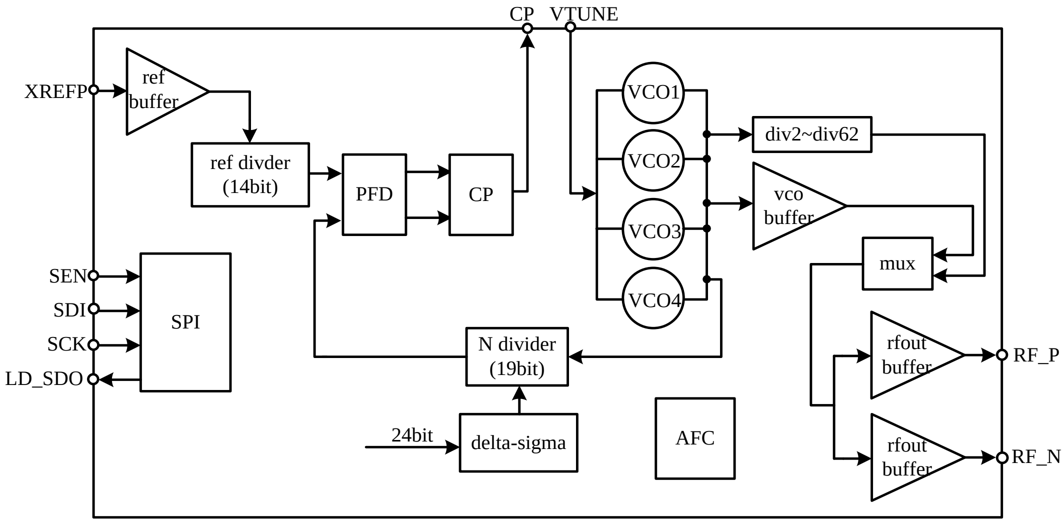


Figure 1 Schematic Block Diagram of XN406 Fractional-N Frequency Synthesizer with Integrated VCO 25MHz-3GHz

Pin Definitions

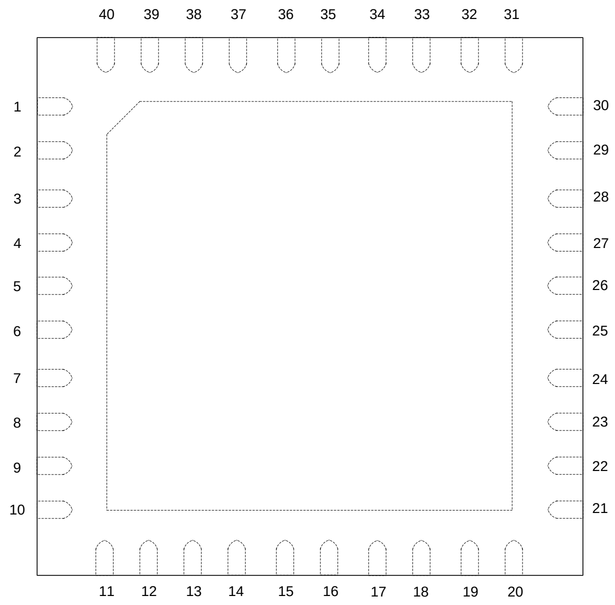


Figure 2 Layout of XN406 Leading-out Terminals (Top View)

S/N	Designation	Function Description	Typical Current
1	AVDD	DC power supply of analog circuit	1.7mA
2	N/C	Not Connect	/
3	VPPCP	Power Supply for charge pump analog section	4.5 mA
4	CP	Charge Pump Output	/
5	N/C	Not Connect	/
6	N/C	Not Connect	/
7	VDDLS	Power Supply for the charge pump digital section	1.2mA
8	N/C	Not Connect	/
9	N/C	Not Connect	/
10	RVDD	Reference Supply	6.8mA
11	N/C	Not Connect	/
12	N/C	Not Connect	/
13	N/C	Not Connect	/
14	N/C	Not Connect	/
15	XRERP	Reference input	/
16	DVDD3V	DC Power Supply for Digital (CMOS) Circuitry (connecting 51Ω resistance to 3.3V power supply during application)	9.4mA
17	CEN	Chip enable (normal operation at high level)	2.7uA (outflow) /0.1uA (inflow)
18	N/C	Not Connect	/
19	N/C	Not Connect	/
20	N/C	Not Connect	/
21	N/C	Not Connect	/
22	N/C	Not Connect	/
23	VTUNE	VCO Varactor. Tuning Port Input	/
24	N/C	Not Connect	/
25	VCC2	VCO Analog Supply 2	114mA
26	N/C	Not Connect	/
27	VCC1	VCO Analog Supply 1	32mA

			(straight-through output)
28	RF_N	RF Negative Output	/
29	RF_P	RF Positive Output	/
30	SEN	PLL Serial Port Enable (CMOS) Logic Input	2.7uA (outflow)/ 0.1uA (inflow)
31	SDI	PLL Serial Port Data (CMOS) Logic Input	2.7uA (outflow)/ 0.1uA (inflow)
32	SCK	PLL Serial Port Clock (CMOS) Logic Input	2.7uA (outflow)/ 0.1uA (inflow)
33	LD_SDO	Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO)	/
34	N/C	Not Connect	/
35	VCCHF	DC Power Supply for Analog Circuitry	3.9mA
36	VCCPS	DC Power Supply for Analog Prescaler	30.9mA
37	N/C	Not Connect	/
38	N/C	Not Connect	/
39	VCCPD	DC Power Supply for Phase Detector	0.9mA
40	BIAS	External bypass decoupling for precision bias circuits.	/

Absolute Maximum Ratings

(All voltages are referenced to GND)

Parameter	Min.	Max.	Unit
VCCHF,VCCPS,VCCPD,AVDD,RVDD	0	3.6	V
VDDLS,VPPCP,VCC1,VCC2	0	5.2	V
Storage temperature Range	-65	150	℃
Maximum Junction temperature		150	℃
Thermal resistance, θ_{JA}		45.3	℃/W
Thermal resistance, θ_{JCtop}		28	℃/W
Thermal resistance, θ_{JB}		15.6	℃/W
Thermal resistance, θ_{JCbot}		6.8	℃/W
Ψ_{JT}		1.0	℃/W
Ψ_{JB}		15.6	℃/W
Lead temperature (10s)		300	℃
Reference input power		+15	dBm
ESD(HBM)	1000		V
ESD(CDM)	400		V

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating temperature range	T_A	-40		+105	℃
VCCHF,VCCPS,VCCPD,AVDD,RVDD	V_{CCL}	3.0	3.3	3.6	V
VDDLS,VPPCP,VCC1,VCC2	V_{CCH}	4.8	5	5.2	V
Reference input power	P_{REF}		6		dBm

Electrical Characteristics

VPPCP, VDDLS, VCC1, VCC2 = 5 V;

RVDD, AVDD, DVDD3V, VCCPD, VCCHF, VCCPS = 3.3 V。

Parameter	Conditions	Min.	Typical	Max.	Unit
RF Output Characteristics					
Output frequency		25		3000	MHz
VCO frequency		1500		3000	MHz
Output Power Characteristics					

RFoutput=2GHz	rf_buf_gain<1:0> = 11 rf_buf_bias<1:0> = 10 rf_out_mode = 0		9		dBm
Harmonic Suppression Characteristics					
RFoutput=2GHz	2nd / 3rd / 4th		-11/-19/-23		dBc
RFoutput=3GHz	2nd / 3rd / 4th		-22/-21/-29		dBc
RFoutput=1.55GHz/62 =25MHz	2nd / 3rd / 4th		-18/-9/-22		dBc
VCO Output Divider Characteristics					
Range of frequency division	1,2,4,6,8,...,62	1		62	
PLL RF Divider Characteristics					
Frequency division range (19bit)	Integer mode	16		524,287	
	Fractional mode	24		524,283	
PLL Reference Input Characteristics					
Reference input range		10		250	MHz
Reference input power range	AC coupling	0		8	dBm
Reference frequency division range (14bit)		1		16,383	dBc
PFD Characteristics					
Range of phase detector frequency	Integer mode	1		100	MHz
	Fractional mode	25		100	MHz
Charge Pump Characteristics					
Charging and discharging current		0.02		2.54	mA
Charging and discharging current stepping	AC coupling		20		uA
Power Supply Voltage Characteristics					
3.3V power supply voltage	AVDD, VCCHF, VCCPS, VCCPD, RVDD,DVDD	3	3.3	3.6	V
5V power supply voltage	VPPCP, VDDLS, VCC1, VCC2	4.8	5	5.2	V
Reference frequency division range (14bit)		1		16,383	
Power Supply Current Characteristics					
3.3V power supply current			65		mA
5V power supply current	Fundamental frequency mode		165		mA
	Frequency division mode /2		200		mA
	Frequency division mode /62		220		mA
VCO Open-loop Phase Noise Characteristics (RFoutput=1.5GHz)					
10 kHz Offset			-92		dBc/Hz
100 kHz Offset			-121		dBc/Hz
1 MHz Offset			-144		dBc/Hz
10 MHz Offset			-160		dBc/Hz
VCO Open-loop Phase Noise Characteristics (RFoutput=1.8GHz)					
10 kHz Offset			-87		dBc/Hz
100 kHz Offset			-118		dBc/Hz
1 MHz Offset			-141		dBc/Hz
10 MHz Offset			-160		dBc/Hz
VCO Open-loop Phase Noise Characteristics (RFoutput=2.3GHz)					
10 kHz Offset			-86		dBc/Hz
100 kHz Offset			-116		dBc/Hz

1 MHz Offset			-139		dBc/Hz
10 MHz Offset			-159		dBc/Hz
VCO Open-loop Phase Noise Characteristics (RFoutput=3GHz)					
10 kHz Offset			-80		dBc/Hz
100 kHz Offset			-110		dBc/Hz
1 MHz Offset			-134		dBc/Hz
10 MHz Offset			-153		dBc/Hz
VCO Tuning Gain Characteristics					
fvco= 1.5GHz	vtune=2.5V		10		MHz/V
fvco= 2GHz	vtune=2.5V		15		MHz/V
fvco= 2.5GHz	vtune=2.5V		16.6		MHz/V
fvco= 3GHz	vtune=2.5V		17		MHz/V
Normalized Phase Noise					
Integer mode			-230		dBc/Hz
Fractional mode			-227		dBc/Hz
1/f noise			-266		dBc/Hz
Spuriousness Characteristics					
Fractional spur (Non-integer boundary)	Phase detector frequency: 61.44MHz, loop bandwidth: 100kHz, Span: within 100MHz		-70		dBc
Integer boundary spur	Phase detector frequency: 61.44MHz, loop bandwidth: 100kHz, offset: 1MHz		-80		dBc
	Phase detector frequency: 61.44MHz, loop bandwidth: 100kHz, offset: 100MHz		-50		dBc
PFD spurious	Phase detector frequency: 61.44MHz, loop bandwidth: 100kHz, $1*f_{pfd}$~$3*f_{pfd}$		-80		dBc

Note: (1) When operating in fractional and integer modes, it is recommended that the charge pump should not be set to HiK mode.

(2) When the product is applied to the electronic system, the offset current of the charge pump shall not exceed 20% of the charging and discharging current.

Typical Characteristic Curves

Unless otherwise specified, T_A=25℃, VCCHF=VCCPS=VCCPD=AVDD= RVDD=DVDD =3.3V, and VPPCP=VDDLS =VCC1=VCC2=5V based on the XN406 test evaluation board.

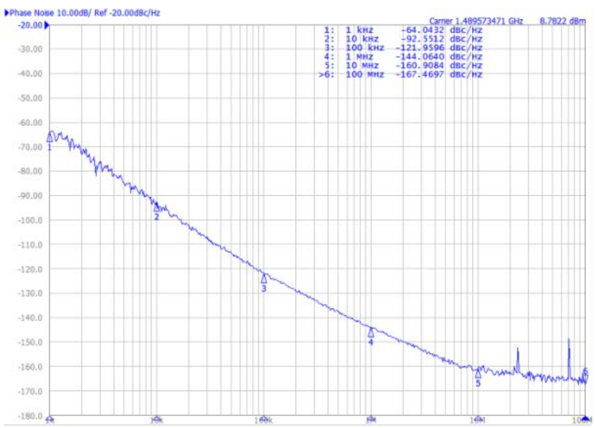


Figure 3 Open-loop Phase Noise (@1.49GHz)

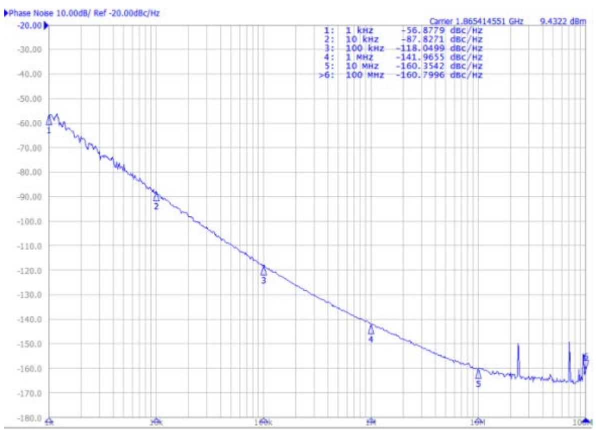


Figure 4 Open-loop Phase Noise (@1.86GHz)

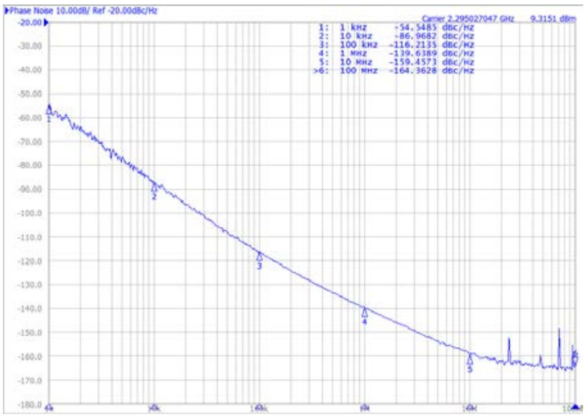


Figure 5 Open-loop Phase Noise (@2.29GHz)

Figure 6 Open-loop Phase Noise (@3.16GHz)

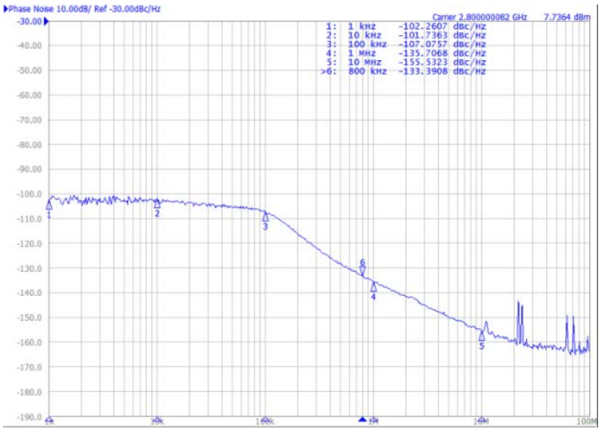


Figure 7 Closed-loop Phase Noise (@2.8GHz)

Figure 8 Closed-loop Phase Noise (@1.795GHz)

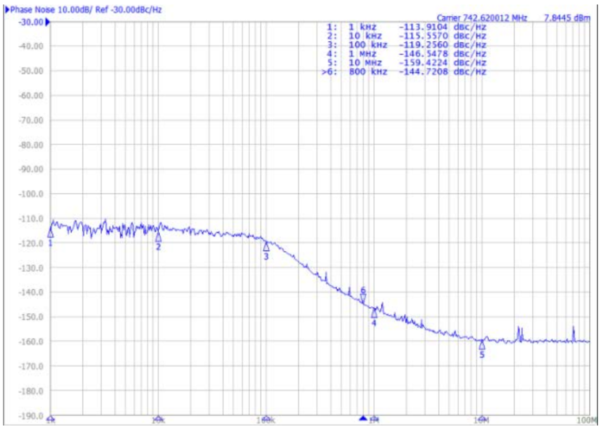


Figure 9 Closed-loop Phase Noise (@742.6MHz)

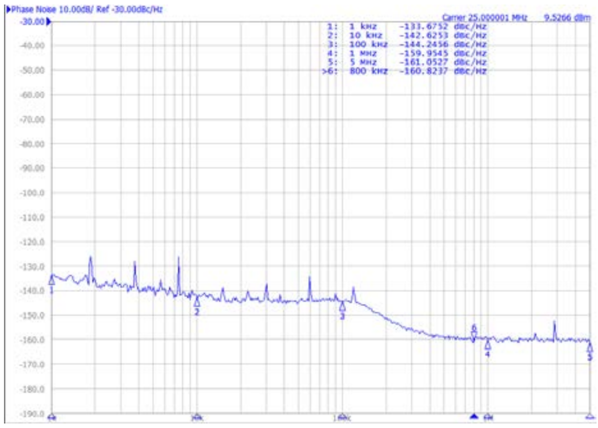


Figure 10 Closed-loop Phase Noise (@25MHz)

Typical Applied Circuits

If only one XN406 is used in the application system, the pin connection relationship is shown in Figure 11. If two or more XN406 are used simultaneously in the system, there is a leakage of VCO oscillation signals at SPI ports between different XN406, especially when multiple XN406 are locked to the same frequency, the same frequency interference between them will deteriorate the near-end phase noise of XN406. It is can be settled by adding a C-R-C low-pass filter circuit to ports SEN, SDI, SCK, and

LD_SDO of the XN406. The application circuit is shown in Figure 12.

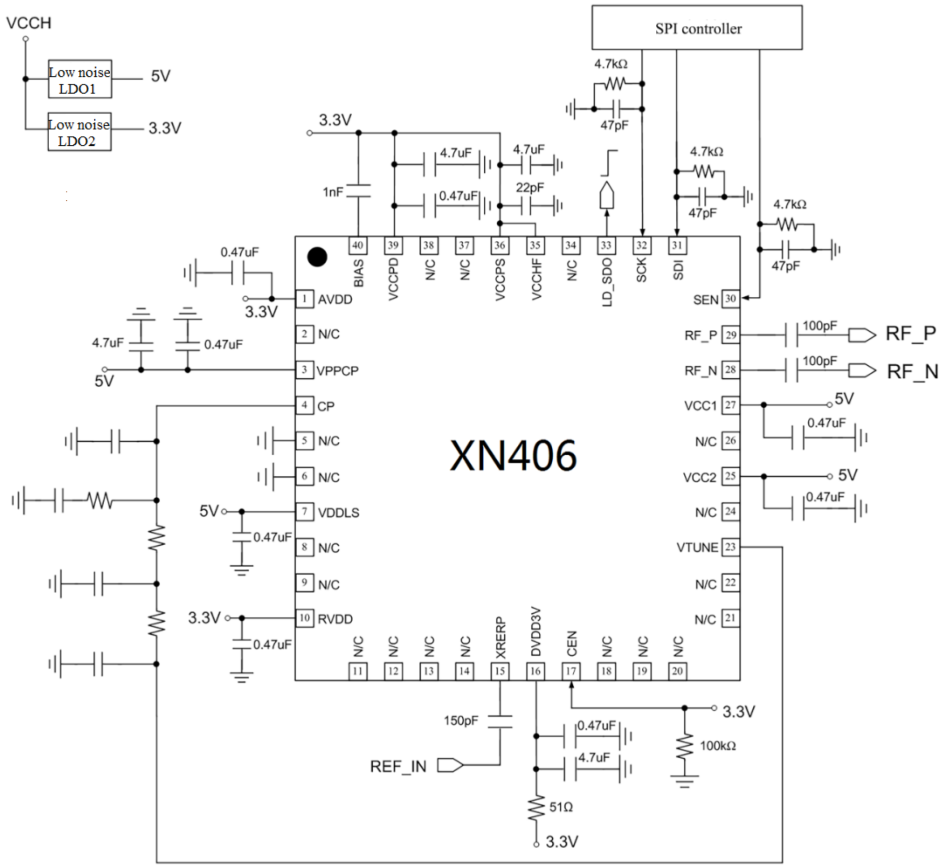


Figure 11 XN406 Typical Application Schematic Diagram (Single-chip Application)

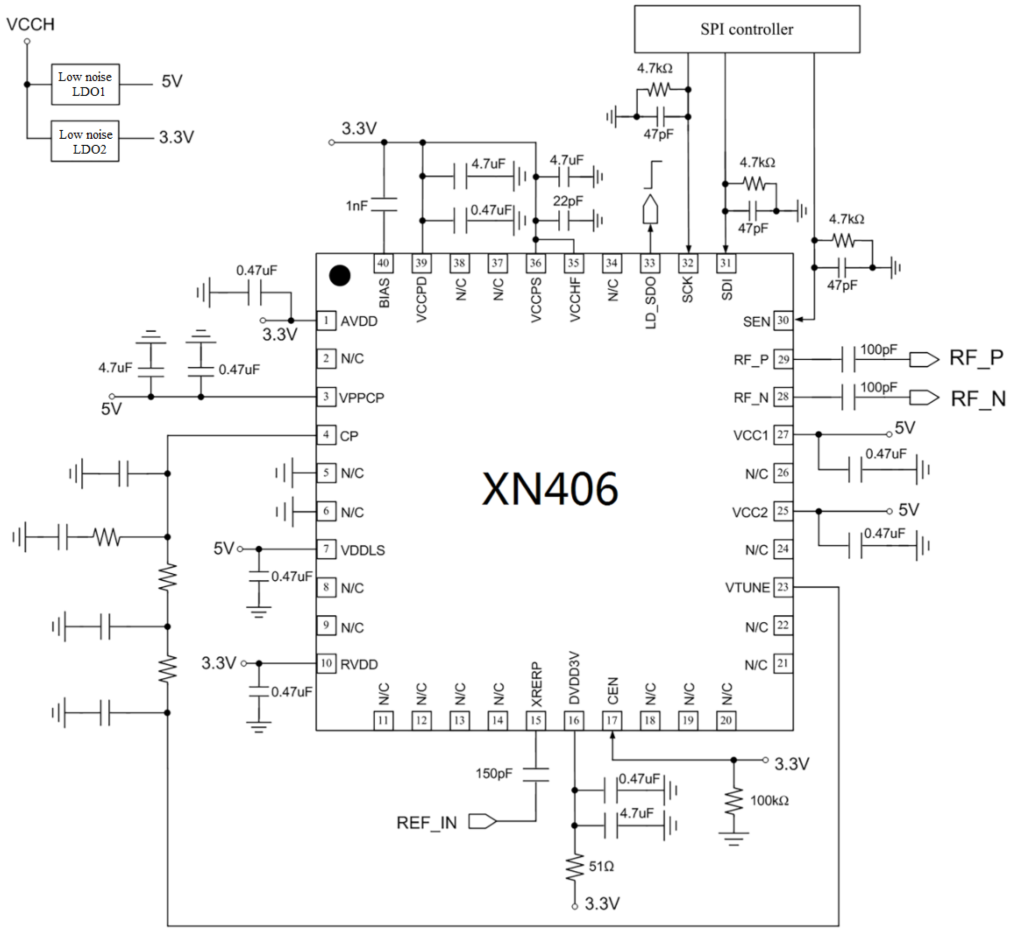


Figure 12 XN406 Typical Application Schematic Diagram (Dual-chip and Multi-chip Application)

Description

Reference Buffer and Reference Divider

The reference buffer is used to connect the path between the external reference source and the reference divider. The reference buffer is equipped with a DC bias circuit. In practical use, the external reference source must be capacitively AC coupled to the reference input XREFP. In order to maintain the high input slew rate, when the input signal frequency is less than 25MHz, it is recommended to select the reference source with relatively square waveform as the input; when the input frequency is greater than or equal to 25MHz, the sine wave or square wave signal can be selected as the input. It should be noted that in order to achieve excellent phase noise performance of baseplate, it is necessary to select a reference source with phase noise better than - 142dBc / Hz at the frequency offset of 1kHz as the input; when the reference input signal power is low, the phase noise in the closed-loop band will deteriorate. It is recommended that the signal power added to the reference port be 0dBm or above.

The reference divider can divide the reference input frequency and support the reference input frequency up to 250MHz. The frequency dividing ratio of the reference divider ranges from 1 to 16383, and the corresponding control register is Reg02h<13:0>.

The reference input circuit inside the XN406 chip is shown in Figures 13 and 14. There is a DC circuit inside the chip, and the resistance of the internal DC power supply port is 210 Ω. It is recommended that you connect to the XREFP pin of the chip after blocking 150pF as shown in Figure 14, and the reference input power should range from 0dBm to 8dBm. If 50Ω matching needs to be considered, the connection can be made as shown in Figure 13, and the corresponding reference input power should range from 6dBm to 14dBm.

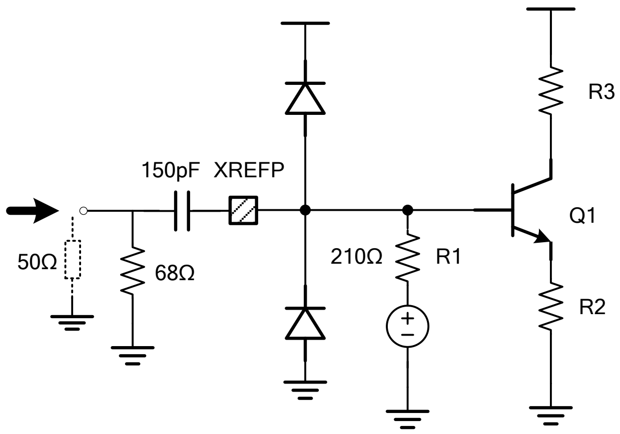


Figure 13 Reference Input Circuit (50Ω matching for peripheral equipment)

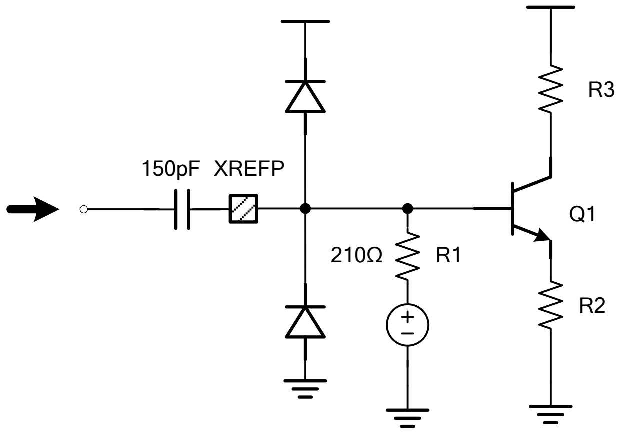


Figure 14 Reference Input Circuit (connection to blocking capacitor)

PFD and CP

The PFD circuit is used to compare the reference channel frequency and the output frequency of the RF divider, convert it into a pulse-width signal and connect it to the charge pump circuit. The active or passive loop filter shall be used when the frequency synthesizer is used with external VCO. When the passive loop filter is used, the Reg 0Bh<4> register shall be configured as "0". The higher the output voltage of the corresponding loop filter, the higher the VCO oscillation frequency. When the active loop filter is used, the Reg 0Bh<4> register shall be configured as "1". Since the connection relationship of the operational amplifier in the active loop filter is negative RF, the final characteristic is the higher the output voltage of the loop filter, the higher the VCO frequency.

The charge pump can operate in non-HiK mode and HiK mode. In the typical application mode, it is recommended that you can adopt non-HiK mode (Reg09<23> is the HiK switch control and the non-HiK mode is set to 0). The range of charging current and discharging current is 20uA to 2.5mA (non-Hik mode), and the range of offset current is 5uA to 635uA. In HiK mode, based on non-HiK mode, the charging current source and the discharging current source add one resistance to the power supply and one resistance to the ground respectively, so the mismatch between the charging current and the discharging current changes obviously with the output voltage.

It should be noted that when this product is used, the offset current of the charge pump cannot exceed 20% of the charging and discharging current.

Configuration of Frequency Dividing Ratio

Assume that the input frequency of a reference buffer is f_{xtal}; the frequency dividing value of a reference divider is R; the integer frequency dividing value of a continuous divider is N; the fractional frequency dividing value is $\frac{Frac+\frac{Extact\_in}{Extact\_mod}}{2^{24}}$; the frequency dividing value of a prescaler is 2^{DIV2_en} (if DIV2_en is "1", the frequency dividing value shall be 2; if DIV2_en is "0", the frequency dividing value shall be 1); and the VCO oscillation frequency is f_{vco} . There is the following equation:

$$f_{vco} = \frac{f_{xtal}}{R} \times 2^{DIV2\_en} \times \left(\mathrm{N} + \frac{Frac + \frac{Exact\_in}{Exact\_mod}}{2^{24}} \right)$$

Where, R value is configured by Reg02h<13:0>, DIV2_en is configured by Reg08h<19>, N is configured by Reg03h<18:0>, and Frac is configured by Reg04h<23:0>. In the imprecise frequency mode, $\frac{Extal\_in}{Extal\_mod}$ = 0 (the imprecise frequency mode is a default mode, and values of the register 0C are 0); in case of the precise frequency mode, you need to configure the register 0C. $\frac{Extal\_in}{Extal\_mod}$ shall be configured as a fractional value which is equivalent to the calculated fractional part.

Taking the phase detector frequency of 61.44MHz and the locking frequency of 1,502MHz as examples, the frequency dividing value is 1502 / 61.44 = 24.446614583333333....... In which the integer frequency dividing value is 24, the fractional frequency dividing value is 0.446614583333333....... And taking the 2^{24} as modulo, the numerator is 0.446614583333×224=7492949.33333.... In the imprecise frequency mode, you shall omit 0.33333... and set Frac to 7492949. At this time, you shall configure the register 04 to 7492949 to obtain the frequency 61.44 × (24 +7492949/224) = 1501.999998779296875MHz. To get an accurate frequency of 1502MHz, you shall set Exact_in (register 0C: byte high 12) and Exact_mod (register 0C: byte low 12) in the precise frequency mode, using the fractional value of

$\frac{Extal\_in}{Extal\_mod}$ which is equivalent to 0.33333... omitted earlier. In the precise frequency mode, $Frac + \frac{Extal\_in}{Extal\_mod} = 7492949 + \frac{1000}{3000}$ = 7492949. 33333..., so you should set Frac to 7492949, Exact_in to 1000 (for hexadecimal 3E8) and Exact_mod to 3000 (for hexadecimal BB8) to be equivalent to 0.33333....

In the precise frequency mode, Exact_in and Exact_mod should be as large as possible, for example, 1000 / 3000 is better than 1 / 3.

Configuration of RF Divider and Frequency Dividing Ratio

The specific architecture of the RF divider path is shown in Figure 15. The prescale unit supports two functions, i.e. /2 and bypass, and the 19bit multi-modulus divider is used to realize continuous frequency dividing ratio control. In the integer frequency dividing mode, there are two frequency dividing ratio ranges in total, and in the fractional frequency dividing mode, there are also two frequency dividing ratio ranges.

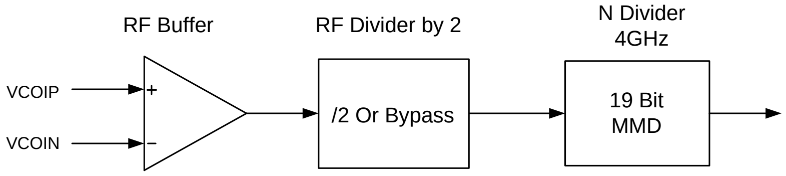


Figure 15 RF Divider Path

If the prescaler is set as straight-through (Reg08h<19> needs to be set as "0"), the operating frequency below 4GHz is supported, and the RF input signal directly enters the 19bit multi-modulus divider, then in this mode, the ratio range of the divider that can be realized is 16 to 524287.

If the prescaler is set as a divider divided by 2 (Reg08h<19> needs to be set to "1"), the operating frequency between 4GHz and 8GHz is supported. After passing the divider divided by 2, the RF input signal enters the 19bit multi-modulus divider. In this mode, the ratio range of the divider that can be realized is 32 to 1048574, and the integer frequency dividing ratio can only be an even number.

In the fractional frequency dividing mode, the frequency dividing ratio contains both integer values and decimal values. Considering the random number interpolation range of Delta-Sigma modulator, the integer value of frequency dividing ratio is narrower than that in the integer frequency dividing mode. Specifically, the lower limit value of integer frequency dividing value set in the previous two modes needs to be processed by - 4 and the upper limit value needs to be processed by + 3. For example, in the prescale straight-through mode, the value of the integer part may range from 20 to 524283 for the fractional frequency dividing mode; the value of the integer part may range from 40 to 1048566 ((20~524283) *2) for the mode of the prescale divided by 2.

Description of Frequency Configuration

Taking the target frequency point 2941.92MHz (outputs of fractional frequency division and fundamental frequency) as an example, the example of the signaling process after power-on is shown in the following table.

Table 1 Example of 2941.92MHz Register Configuration
(outputs of fractional frequency division and fundamental frequency)

Condition: Reference frequency: 122.88MHz, phase detector frequency: 61.44MHz				
Signaling sequence	Register address	Register data	Description	Remarks
1	0x01	0x02		
2	0x02	0x02	Reference divider divided by 2 (This register value can be modified if it is operating in the reference straight-through mode)	
3	0x05	0x0F88	VCO register address is VCO 01H	
4		0xE090	VCO register address is VCO 02H	
5		0x3898	VCO register address is VCO 03H	
6		0xA0A0	VCO register address is VCO 04H	
7		0x5528	VCO register address is VCO 05H	
8		0x7FB0	VCO register address is VCO 06H	
9	0x07	0x14D		
10	0x08	0xC1BEFF		
11	0x09	0x5AF264		
12	0x0A	0x2041	The AFC comparison cycle is switched to 1000	
13	0x0B	0x7C021		
14	0x0F[1]	0x81	Single XN406: When reading the data, LD_SDO outputs the register content read, and outputs the indication of phase-locked detection at the rest of the time	LD_SDO configuration value when used alone
14’	0x0F[1]	0x01	XN406 output is connected with other chips in parallel. When reading the data, LD_SDO outputs the register content read, and the output at the rest of the time are in a high-impedance state to avoid level conflict	LD_SDO configuration value when connected with other chip outputs in parallel
15	0x06	0x200B42	Switching to the first-order fractional mode	
16	0x05	0x5F00	Manual segment selection control VCO output frequency	Lowest segment of sub-high VCO
17	0x03	0xEF	Insert value N (0xC8 | 0x2F)	Results performed or calculated by integer frequency dividing values before and after insertion
18	0x03	0x2F	Configuration of integer frequency dividing part	

19	0x04	0XE20000	Fractional part, and triggering automatic segment finding	
Waiting time[2]				
20	0x06	0x200B4A	Fractional algorithm is configured as third order	
备注： Notes: [1]Reg0F<7:6> combination description: 00: When reading the data, LD_SDO outputs the register content read, and the output at the rest of the time is in a high-impedance state; 01: When reading the data, LD_SDO outputs the selected data of gpo_select (register 0F: byte low 5), and the output at the rest of the time is in a high-impedance state; 10: When reading the data, LD_SDO outputs the register content read, and outputs the selected data of gpo_select at other times; 11: LD_SDO always outputs selected data of gpo_select; [2] The time of AFC segment selection is about 8000 × T_{ref} (phase detector frequency cycle)				

Steps 15~20 above shall be repeated if frequency hopping with fractional frequency point as a target is required after register configuration.

Taking the target frequency point 2800MHz (outputs of integer frequency division and fundamental frequency) as an example, the example of the signaling process after power-on is shown in the following table.

Table 2 Example of 2800MHz Register Configuration
(outputs of integer frequency division and fundamental frequency)

Condition: Reference frequency: 20MHz, phase detector frequency: 20MHz				
Signaling sequence	Register Address	Register Data	Description	Remarks
1	0x01	0x02		
2	0x02	0x01		
3	0x05	0x0F88	VCO 寄存器地址 VCO 01H VCO register address is VCO 01H	
4		0xE090	VCO 寄存器地址 VCO 02H VCO register address is VCO 02H	
5		0x3898	VCO 寄存器地址 VCO 03H VCO register address is VCO 03H	
6		0xA0A0	VCO 寄存器地址 VCO 04H VCO register address is VCO 04H	
7		0x5528	VCO 寄存器地址 VCO 05H VCO register address is VCO 05H	
8		0x7FB0	VCO 寄存器地址 VCO 06H VCO register address is VCO 06H	
9	0x07	0x14D		
10	0x08	0xC1BEFF		
11	0x09	0x1AF264		
12	0x0A	0x2041		
13	0x0B	0x7C061		
14	0x0F	0x81	Single XN406: When reading the data, LD_SDO outputs the register	LD_SDO configuration

			content read, and outputs the indication of phase-locked detection at the rest of the time	value when used alone
14’	0x0F	0x01	XN406 output is connected with other chips in parallel. When reading the data, LD_SDO outputs the register content read, and the output at the rest of the time are in a high-impedance state to avoid level conflict	LD_SDO configuration value when connected with other chip outputs in parallel
15	0x03	0xCC	Insert value N (0xC8 | 0x8C)	Results performed or calculated by integer frequency dividing values before and after insertion
16	0x06	0x2003CA	Switching to integer mode	
17	0x03	0x8C	Integer part, and triggering automatic segment finding	

When the frequency hopping is between integer frequency points, the steps 15~17 above shall be changed as follows:

Table 3 Register Configuration Sequence of Frequency Hopping between Integer Frequency Points

15	0x0A	0x2841	Turn off AFC	Avoid starting the automatic segment selection process after inserting the N' value
16	0x03	N’	Insert value N' (N1 | N2)	N' is the result performed or calculated by integer frequency dividing values before and after insertion, N1 is the integer frequency dividing value of the previous frequency point, and N2 is the integer frequency dividing value of the target frequency point
17	0x0A	0x2041	Turn on the AFC	Recovery of AFC function
18	0x03	N2	Integer part, and triggering automatic segment finding	

During the frequency hopping of XN406 from *f*1 (the integer part corresponding to the RF frequency dividing ratio is N1) to *f*2 (the integer part corresponding to the RF frequency dividing ratio is N2), if *f*1 / N2 ≥ 100MHz, the input clock frequency of sigma-delta modulator will exceed the design value of 100MHz, resulting in abnormal segment selection of AFC. In order to avoid this state, in the actual frequency hopping process, manual configuration of the VCO segment shall be used to control the output frequency, and a value N' (N' = N1 | N2, binary values of N1 and N2 are taken by bit) shall be inserted to avoid abnormal RF frequency division clock output (affecting AFC). The following operation steps must be followed:

(1) Reg06=0x200B42 (bypass=0, frac_en=1, switching to first-order fractional mode)

(2) Reg05=0x5F00 (manually adjusting the VCO segment to the lowest segment of sub-high VCO to control the VCO output frequency)

(3) Reg03=N' (inserting transition value N)

(4) Reg03=N (target integer frequency dividing value)

(5) Reg04=F (target fractional frequency dividing value, triggering AFC segment selection)

(6) Reg06=0x200B4A (switching to third-order fractional mode)

When the frequency point is switched by the above method, the integer value N of the RF frequency dividing ratio shall not be less than 24.

Configuration Timing Description of Power-on and Power-off SPI

In order to ensure the normal operation of the circuit, the power-on time shall be less than or equal to 30ms. From the power-on time, it is necessary to wait for ≥1s to configure the XN406 register, as shown in Figure 16. Meanwhile, in order to ensure the normal operation of the circuit when it is powered on again after power failure, the duration of 0 V after power supply voltage discharge should be greater than or equal to 30 ms, as shown in Figure 17. In addition, during the application of the circuit, the 3.3V and 5V power supplies shall be powered on first, and then the reference input signal shall be added; or the reference input signal shall be provided when the 3.3V and 5V power are applied.

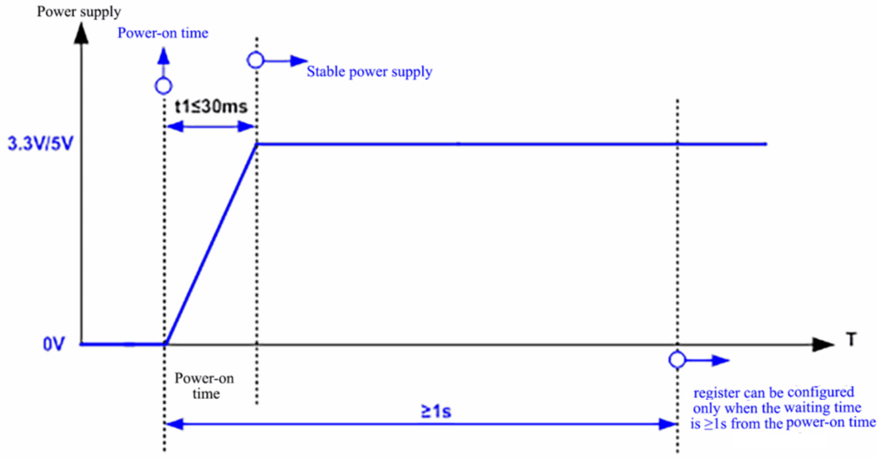


Figure 16 Power-on Schematic Diagram

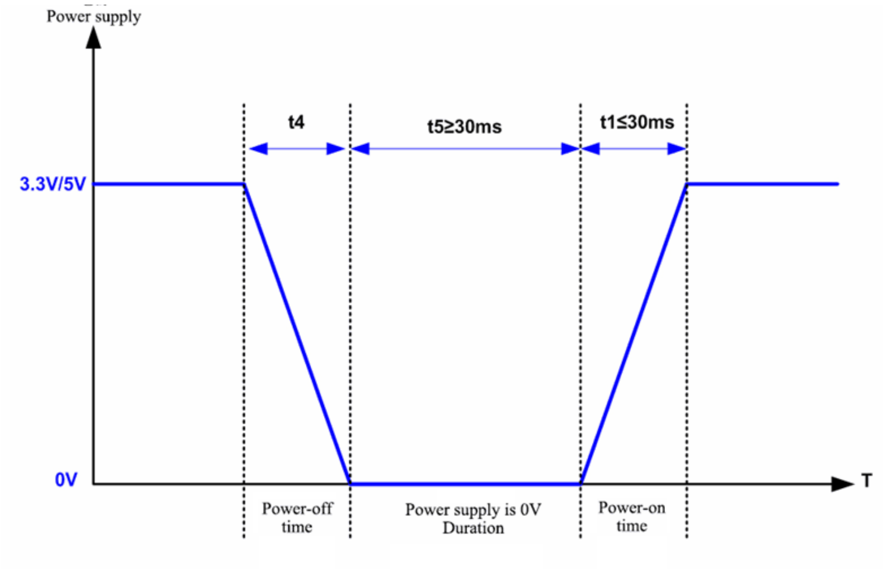


Figure 17 Schematic Diagram of Secondary Power-on

Description of Power Supply

The frequency synthesizer of this product is a supply-sensitive device. In order to achieve the optimal FOM characteristics, it is recommended to select LDO with low output noise for power supply. At the same time, star connection should be considered when PCB layout in different power domains (RF, analog and digital), and decoupling capacitor should be connected near the chip power pin.

Control Interface

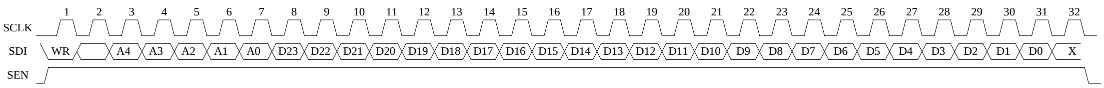
XN406 is formed by chip 1 (PFD chip) and chip 2 (VCO chip).

(1) Serial port control timing of chip 1 (PFD chip)
The legacy mode and open mode are supported.

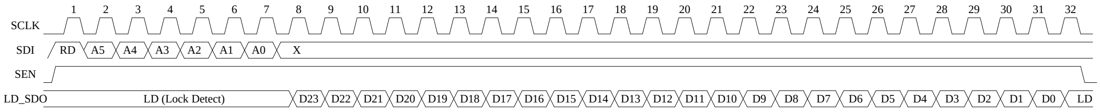
SPI mode selection depends on the timing of SEN and SCLK when the chip is powered on. When the rising edge of SEN appears first, the legacy mode is set for the chip; when the SCLK rising edge appears first, the open mode is set. No matter which mode is selected, it can only be switched after power on again. During chip power-on, the serial control interface output by the upper computer shall be kept at low level.

In the legacy mode, the SEN signal enables an SPI operation. When the SEN signal has a high level, SPI master starts accessing the XN405 chip through the clock (SCLK) and data (SDI, SDO) ports. The frame data is arranged in a high bit first (msb). The MSB is the reading and writing sign (high indicates the reading operation and low indicates the writing operation), the next 6bit is the register address, and the last 24bit is the data. During the communication between SPI master and XN406, the master updates and samples data through the falling edge, and the slave samples and outputs data through the rising edge. After the access operation is completed, SEN changes from high level to low level. Reading and writing are shown in Figure 18.

In the open mode, SEN is used as the data latch signal, and the clock cooperates with the data input (SDI) to write the data into the shift register first. When the rising edge of SEN appears, the designated register is updated. In open mode, the data format is different from the legacy mode, in which, in addition to the data information and register address information, the chip address information (A2~A0) is also included. Therefore, the open mode supports the control of multiple chips. It should be noted that in open mode, the address of the register read is corresponding to the bytes low 5 of the register 0. Therefore, two frames of SPI operation are required for data reading. One frame is written into the register 0 to update the reading address and one frame is used to obtain the target register data. Reading and writing are shown in Figure 19.

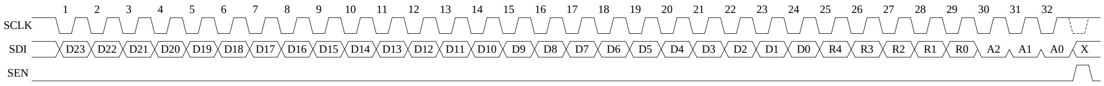


Writing Timing

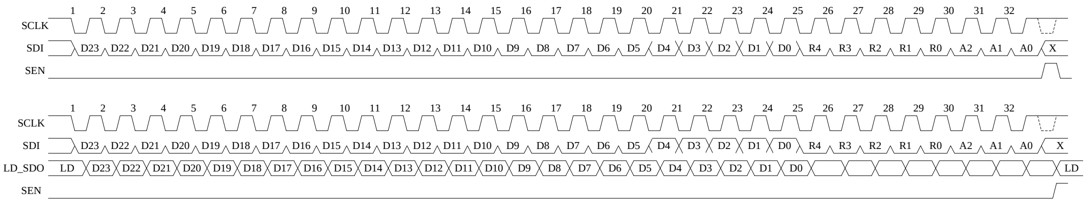


Reading Timing

Figure 18 Reading and Writing Timing in Legacy Mode



Writing Timing



Reading Timing

Figure 19 Reading and Writing Timing in Open Mode

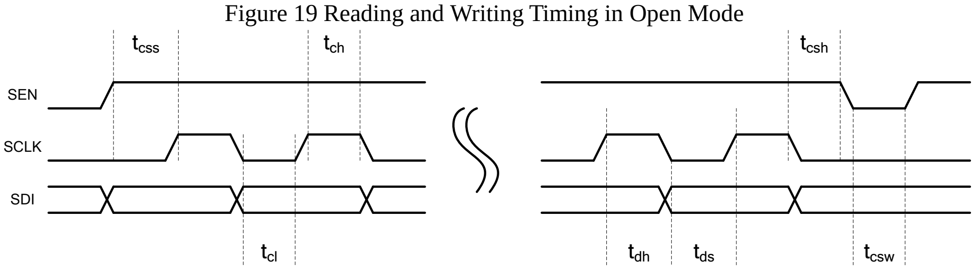


Figure 20 Interface Timing in Legacy Mode

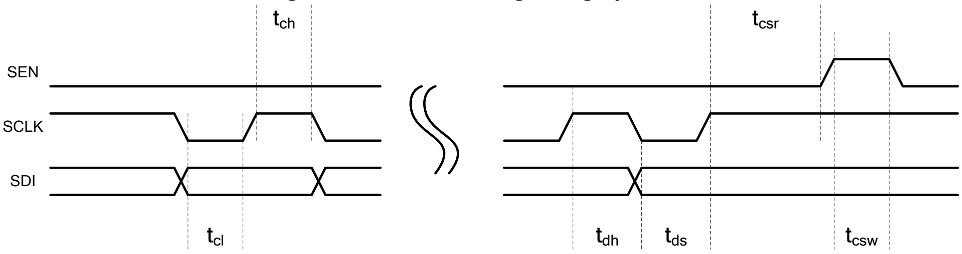


Figure 21 Interface Timing in Open Mode

SPI timing requirements:

Symbol	Parameter	Min.	Unit
t_{css}	SEN rising edge to the first rising edge of SCLK	10	ns
t_{ds}	Data establishment time	10	ns
t_{dh}	Data maintance time	10	ns
t_{ch}	Clock duration at high level	25	ns

t_{cl}	Clock duration at low level	25	ns
t_{csh}	Last falling edge of SCLK to SEN falling edge	0	ns
t_{csr}	Last rising edge of SCDK to SEN rising edge	1	clock
t_{csw}	SEN duration at fixed level	1	clock

(2) Serial port control timing of chip 2 (VCO chip)

Only writing is allowed. When the control object is VCO chip, the register address of the PFD chip is 5. The VCO chip register data, address and ID number are 16 bits in total, so the next 8 bits of data are 0. After that, 9 bits are for the VCO chip register data, then 4 bits are for the VCO chip register address, and the last 3 bits are 0. Its timing operation is shown in Figure 22.

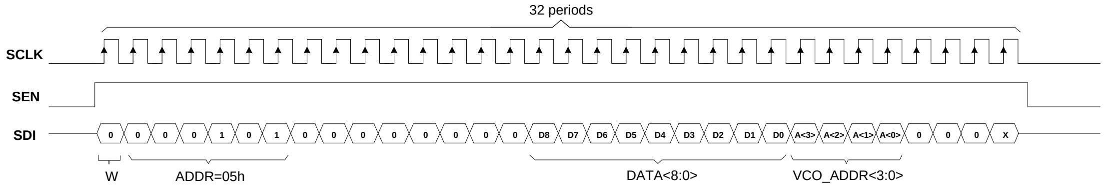


Figure 22 VCO Chip Writing Timing Diagram (External SPI)

This operation is reflected in the VSPI interface as shown in the figure below.

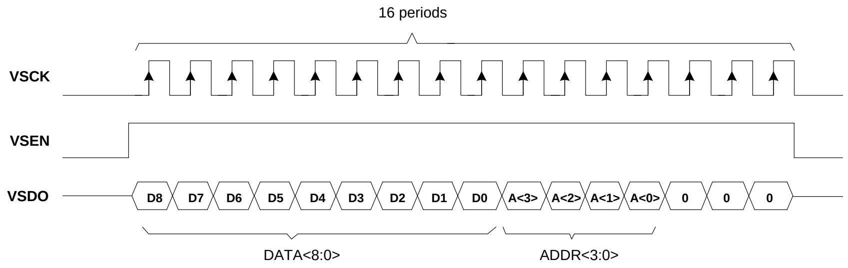


Figure 23 VCO Chip Writing Timing Diagram (VSPI)

Register Definitions of PFD Chip

Reg 00h ID register (534744h)

Bit	Name	Type	Default value	Description
<23:0>	Chip_ID	RO	0101 0011 0100 0111 0100 0100	Chip ID: 534744h. This register prohibits writing data

Reg 01h register with chip enable control (000002h)

Bit	Name	Type	Default value	Description
<23:2>	reserved	R/W	0	Reserved
<1>	rst_chipen_from_spi	R/W	1	Chip SPI enable: When regx01<0>=0, regx01<1> is 1, the chip enables; when regx01<1> is 0, the chip is turned off.
<0>	rst_chipen_pin_select	R/W	0	When the register is configured as 1, the chip enable is realized through CEN. If the CEN is 1, the chip enables; if the CEN is 0, the chip is turned off. When the register is configured as 0, chip enable is controlled via Reg01[1].

Reg 02h register with reference frequency dividing value control (000001h)

Bit	Name	Type	Default value	Description
<23:14>	reserved	R/W	00	Reserved

			0000 0000	
<13:0>	rdiv<13:0>	R/W	00 0000 0000 0001	Reference frequency dividing value setting, valid when Reg08[3]=1

Reg 03h register with control of integer frequency dividing value of RF divider (0000C8h)

Bit	Name	Type	Default value	Description
<23:19>	reserved	R/W	0 0000	Reserved
<18:0>	Intg<18:0>	R/W	000 0000 0000 1100 1000	Integer frequency dividing value setting

Reg 04h register with control of fractional frequency dividing value of RF divider (000000h)

Bit	Name	Type	Default value	Description
<23:0>	frac<23:0>	R/W	0000 0000 0000 0000 0000 0000	Fractional frequency dividing value setting

Reg 05h VCO SPI control register (000000h)

Bit	Name	Type	Default value	Description
<15:14>	VCO select	R/W	00	Sub-VCO selection. 00, minimum frequency of VCO. 11:maximum frequency of VCO
<13>	reserved	R/W	0	Reserved
<12:8>	VCO caps	R/W	0 0000	VCO segment selection 0 0000:the lowest 1 1111:the highest
<7>	Open/close loop	R/W	0	VCO tuning open and closed loop control positions. 0: Closed loop 1: Open loop
<6:3>	VCO Subsystem register address	R/W	0000	VCO chip register address
<2:0>	VCO Subsystem_ID	R/W	000	VCO chip ID

Reg 06h SD configuration register (200B4Ah)

Bit	Name	Type	Default value	Description
<21>	auto_clock_config	R/W	1	Reserved
<11>	frac_en	R/W	1	0: Turn off fractional frequency division function 1: Turn on fractional frequency division function
<10>	reserved	R/W	0	Reserved
<9>	reserved	R/W	1	Reserved
<8>	AutoSeed	R/W	1	1: As long as the fractional register is written, the modulator seed is loaded. 0: When the fractional register value changes, the initial phase of the modulator is obtained from the previous state.
<7>	bypass_frac	R/W	0	Sigma-delta modulator outputs the signal of bypass control, 0: Non-bypass modulator; 1: Bypass modulator, under integer mode;
<6:4>	reserved	R/W	100	Reserved
<3:2>	sd_sel<1:0>	R/W	10	Fractional frequency division algorithm selection:

				00: First-order 01: Second-order 10: MASH
<1:0>	seed	R/W	10	Seed selection in fractional mode. 00: 0 01: 1 02: B29D08h 03: 50F1CDh The selected seed is written into the modulator only when the frequency changes and Reg06h[8]=1

Reg 07h configuration register with phase-locked detection (00014Dh)

Bit	Name	Type	Default value	Description
<14>	Lock Detect Window type	R/W	0	Selection of phase-locked detection mode 0: Counting mode 1: Window mode
<13>	Auto Relock – One Try	R/W	0	0: Do not restart the AFC after unlocking 1: Trying to re-lock if phase lock fails
<12>	reserved	R/W	0	Reserved
<11:10>	LD Digital Timer Freq Control	R/W	00	Counter speed control under the window mode of phase-locked detection. 00: The fastest 11: The slowest
<9:7>	LD Digital Window duration	R/W	010	Window duration under the window mode of phase-locked detection unit 0: 5.5ns 1: 5.5ns 2: 8.7ns 3: 15.4ns 4: 27.8ns 5: 52.2ns 6: 100.7ns 7: 197ns Condition: $T_{offset}<T_{win}<T_{PFD}$
<6>	reserved	R/W	1	Reserved
<5:4>	reserved	R/W	00	Reserved
<3>	Enable Internal Lock Detect	R/W	1	The phase-locked detection unit is enabled. 0:off 1:operating
<2:0>	lkd_wincnt_max		101	For multiplex register, the default mode of phase-locked detection is counting mode 0: 16 (window mode) /16 (counting mode) 1: 32 (window mode) /32 (counting mode) 2: 96 (window mode) /64 (counting mode) 3: 256 (window mode) /256 (counting mode) 4: 512 (window mode) /512 (counting mode) 5: 2048 (window mode) /2048 (counting mode) 6: 8192 (window mode) /8192 (counting mode) 7: 65535 (window mode) /65520 (counting mode)

Reg 08h register with analog circuit enable control (C1BEFFh)

Bit	Name	Type	Default value	Description
<23>	Reserved	R/W	1	Reserved
<22>	Rdiv_en	R/W	1	The R counter is enabled. 0, off; 1, operating
<21>	Hi Frequency Reference	R/W	0	When XTAL > 200 MHz, it is set to 1
<20>	Reference ouput limiter	R/W	0	It is set to 0
<19>	8GHz Divide by 2 En	R/W	0	Prescaler divided by 2 of RF divider is enabled. 0:off 1:on
<18>	Reserved	R/W	0	Reserved. It is set to 0
<17:15>	Div Resync Bias /En	R/W	011	RF divider synchronization unit current control code (LSB is 0, off; for other values, only 2-byte high

				control is valid) 0: off 1: Minimum current, ... 7: Maximum current
<14:12>	EtoC Bias /En	R/W	011	RF divider current control code (LSB is 0, off; for other values, only 2-byte high control is valid) 0: Off 1: Minimum current, ... 7: Maximum current
<11>	Charge Pump Internal Opamp enable	R/W	1	The built-in operational amplifier of the charge pump is enabled. 0:off 1:operating It is set to 1
<10>	VCO Buffer and Prescaler Bias Enable （PRE EN）	R/W	1	The Bias of the RF divider is enabled. 0:off 1:operating
<9>	Prescaler Clock enable	R/W	1	Digital counter clock is enabled. 0:off 1:on
<8>	reserved	R/W	0	Reserved
<7>	VCO_Div_Clk_to_dig_en	R/W	1	VCO frequency division clock output to digital
<6>	reserved	R/W	1	Reserved
<5>	GPO/LDO/SDO_pad_en	R/W	1	Pin LD_SDO is enabled. 0: Pin LD_SDO output is in a high-impedance state 1: When RegFh[7]=1, pin LD_SDO keeps output When RegFh[7]=0, the pin LD_SDO output is in a high-impedance state when the chip is not selected, which is used when multiple chip output ports are shared
<4>	vcobuf_en	R/W	1	VCO path RF BUFF is enabled. 0:off 1:operating
<3>	refbuf_en	R/W	1	Reference path RF BUFF is enabled. 0:off 1:operating
<2>	PD_en	R/W	1	PFD is enabled. 0:off 1:operating
<1>	cp_en	R/W	1	CP is enabled. 0:off 1:operating
<0>	bias_en	R/W	1	The charge pump reference bias is enabled. 0:off 1:operating

Reg 09h register with charge pump control (403264h)

Bit	Name	Type	Default value	Description
<23>	HiKcp	R/W	0	Charging and discharging mode of the charge pump. 0:off 1:on
<22>	Offset DN enable	R/W	1	The Offset DN is enabled. It is recommended to set it to 1 in fractional mode and 0 in other modes
<21>	Offset UP enable	R/W	0	It is recommended to set it to 0
<20:14>	Offset Current	R/W	0 0000 00	Control code of charge pump offset current 0d = 0 µA 1d = 5 µA 2d = 10 µA ...

				127d = 635 μA
<13:7>	CP UP Gain	R/W	11 0010 0	Control code of charge pump charging current 0d = 0 μA 1d = 20 μA 2d = 40 μA ... 127d = 2.54mA
<6:0>	CP DN Gain	R/W	110 0100	Control code of charge pump discharging current 0d = 0 μA 1d = 20 μA 2d = 40 μA ... 127d = 2.54mA

Reg 0Ah AFC control register (002205h)

Bit	Name	Type	Default value	Description
<17>	Cnt_delay	R/W	0	0: Waiting for 8 reference cycles after switching VCO 1: No waiting after switching VCO
<16>	Force RDivider Bypass	R/W	0	Forced bypass reference divider. 0:no bypass 1:bypass
<15>	Xtal Falling Edge for FSM	R/W	0	The falling edge of the clock is used to drive the AFC
<14:13>	FSM/VSPI Clock Select	R/W	01	Clock frequency division setting of AFC and VSPI 0: Reference clock 1: Reference clock / 4 2: Reference clock / 16 3: Reference clock / 32
<12>	No VSPI Trigger	R/W	0	VSPI sending is not triggered after writing the 05 register (VCO chip is configured) 0:Trigger sending 1:Do not trigger sending
<11>	Bypass VCO Tuning	R/W	0	Select the VCO and its child segment sources 0: Configuration through SPI (Reg05) and AFC; 1: Configuration of VCO only through SPI (Reg05)
<10>	reserved	R/W	0	Reserved
<9:8>	reserved	R/W	10	Reserved
<7:6>	Wait State Set Up	R/W	00	Waiting for 100 VSPI clock cycles after switching the VCO and its child segment (this clock is determined by Reg0A<14:13>) 0: Waiting after the first switch 1: Waiting after the first two switches 2: Waiting after the first three switches 3: Waiting after the first four switches
<5:3>	VCO Curve Adjustment	R/W	000	Reserved
<2:0>	Vtune Resolution	R/W	101	AFC counting cycle 0:512 1:1000 2:8 3:16 4:32 5:64 6:128 7:256

Reg 0Bh register with offset and enable control (0F8061h)

Bit	Name	Type	Default value	Description
<22>	Reset delay div	R/W	0	Delayed reset of the RF divider
<21:20>	Pulse Width	R/W	00	Output pulse width control of the RF divider

	/Divider Pulse _sel			
<19>	Reserved	R/W	1	Reserved
<18:17>	MCounter Clock Gating	R/W	11	M counter clock gating 0: M Counter closed 1: N<128 2: N< 1023 3: All Clocks ON
<16:15>	CP Internal OpAmp Bias	R/W	11	Reserved
<14:12>	PS Bias	R/W	000	Current control of RF divider
<11>	Force CP MId Rail	R/W	0	The charge pump is forced to output to the intermediate voltage (for test only)
<10>	Force CP DN	R/W	0	The charge pump is forced to set in a discharging mode (for test only)
<9>	Force CP UP	R/W	0	The charge pump is forced to set in a charging mode (for test only)
<8:7>	CSP Mode	R/W	00	Reserved
<6>	PD_dn_en	R/W	1	PFD DN output is enabled. 0:off 1:operating
<5>	PD_up_en	R/W	1	PFD UP output is enabled. 0:off 1:operating
<4>	pd_phase_sel	R/W	0	PFD polarity selection 0: VCO and loop filter with positive polarity (default) 1: VCO and loop filter with negative polarity
<3>	Short PD Inputs	R/W	0	Effective control bit of PFD input signal
<2>	Reserved	R/W	0	Reserved
<1:0>	PD_del_sel	R/W	01	Delayed control bit of PFD deadband (recommended to be set to 01)

Reg 0Ch register with precise frequency control (000000h)

Bit	Name	Type	Default value	Description
<23:12>	Exact_in	R/W	0000 0000 0000	Accurate frequency division mode, numerator
<11:0>	Exact_mod	R/W	0000 0000 0000	Accurate frequency division mode, denominator

Reg 0Fh GPO control register (000001h)

Bit	Name	Type	Default value	Description
<15>	dbuff_en	R/W	0	Dual buffer enable bit of frequency dividing value is highly effective. 1: In integer mode (Reg06<7> =1), the integer frequency dividing value is updated to the divider immediately after writing Reg03 to make the integer frequency division effective directly; in fractional mode (Reg06<7> =0), the integer frequency dividing value and the fractional frequency dividing value are updated to the divider only after writing Reg04 (fractional frequency dividing value). 0: The integer frequency dividing value is directly updated to the divider after writing Reg03.
<14>	reserved	R/W	0	Reserved

<13>	reserved	R/W	0	Reserved
<12>	reserved	R/W	0	Reserved
<11>	Sd_random enable	R/W	0	0:Random number closed 1:Random number opened
<10>	reserved	R/W	0	Reserved
<9>	reserved	R/W	0	Reserved
<8>	reserved	R/W	0	Reserved
<7>	LDO Driver Always On	R/W	0	(In case of Reg08<5>=1) 1: Keep driving the LD_SDO port 0: The LD_SDO port is driven in the SPI reading cycle, and is in the high-impedance state at the rest of the time
<6>	Prevent Automux SDO	R/W	0	1: Select GPO_data as output 0: Select the register data as the output during SPI reading cycle, and use GPO_data as the output for the rest of the time
<5>	GPO Test Data	R/W	0	1:GPO test data
<4:0>	gpo_select	R/W	0 0001	Signal selection 0: Data from Reg0F[5] 1: Phase-locked detection output 3: Phase-locked detection window output 4: Ring oscillator frequency output under window mode of phase-locked detection 8: Reference buffer output 9: Reference frequency division output 10: RF divider output 11:Clock of sigma-delta modulator 13:VCO SPI clock 14:VCO SPI enable signal 15:VCO SPI data 16:PFD DN output 17:PFD UP output 24:Reset signal of RF divider 2, 7, 12, 25:0 5-6, 18-23, 26-31: NC
bit<7:6> description: 00: When reading the data, LD_SDO outputs the register content read, and the output at the rest of the time is in a high-impedance state; 01: When reading the data, LD_SDO outputs the selected data of gpo_select (register 0F: byte low 5), and the output at the rest of the time is in a high-impedance state; 10: When reading the data, LD_SDO outputs the register content read, and outputs the selected data of gpo_select at other times; 11: LD_SDO always outputs selected data of gpo_select				

Reg 10h VCO segment selection and tuned read-only register (000000h)

Bit	Name	Type	Default value	Description
<10:9>	Reserved	R	00	Reserved
<8:1>	VCO Switch setting	R		VCO segment selection
<0>	AutoCal busy	R		Automatic segment selection in progress

Reg 11h Invalid register (007FFFh)

Reg 12h Locked read-only register

Bit	Name	Type	Default Value	Description
<1>	Lock Detect	R		Lock detection
<0>	Reserved	R	0	Reserved

Reg 13h Invalid register (000000h)

VCO Chip Register Definitions

Reg 00h (020h)

Bit	Name	Type	Default value	Description
<8:7>	vco_sel<1:0>	W	00	VCO selection: 11:VCO with the lowest frequency; 00:VCO with the highest frequency
<6>	spare	W	0	
<5:1>	cs<4:0>	W	10000	Selection of VCO segment code: 1 1111: Lowest frequency segment 0 0000: Highest frequency segment
<0>	tune_sel	W	0	VCO tune voltage selection. 0: Tune voltage is selected as the output of the loop filter 1: Tune voltage is selected as the internal positive temperature voltage for VCO tuning segment selection. 0： close loop 1: Open loop

Reg 01h (01Fh)

Bit	Name	Type	Default value	Description
<8:5>	spare	W	0000	
<4>	en_divn	W	1	Div is enabled: 0: off 1: operating
<3>	en_vco_buf	W	1	vco_buf is enabled: 0: off 1: operating
<2>	en_rf_buf	W	1	rf_buf is enabled: 0: off 1: operating
<1>	en_pll_buf	W	1	pll_buf is enabled: 0: off 1: operating
<0>	en_vco_sub	W	1	vco_sub is enabled: 0: off 1: operating

Reg 02h (0C1h)

Bit	Name	Type	Default value	Description
<8>	div_gain	W	0	Divider output gain control. 0: Low gain 1: High gain
<7:6>	rf_buf_gain<1:0>	W	11	rf_buf gain control. 00: Minimum gain 11: Maximum gain
<5:0>	div<5:0>	W	000001	Frequency dividing ratio control of divider. 0: Mute 1: Fo 2, 3: Fo/2 4, 5: Fo/4 6, 7: Fo/6;…… 60, 61: Fo/60 62, 63: Fo/62

Reg 03h (051h)

Bit	Name	Type	Default value	Description
<8:7>	spare	W	00	Reserved

<6:5>	cal_vol_slope<1:0>	W	10	vco_segment voltage slope control
<4:3>	rf_buf_bias<1:0>	W	10	rf_buf bias current control
<2>	Manual RFO Mode	W	0	Output control mode. 0: Automatic control 1: Manual control
<1>	pd_rf_buf_core	W	0	rf_buf_core operating control. 0: Operating 1: Off
<0>	rf_out_mode	W	1	rf_out output mode control. 0: Fundamental frequency output 1: Reserved

Reg 04h (0C9h)

Bit	Name	Type	Default value	Description
<8:7>	cal_vol<1:0>	W	01	vco_segment voltage control
<6:5>	vco_buf_bias<1:0>	W	10	vco_buf bias current control
<4:3>	pll_buf_bias<1:0>	W	01	pll_buf bias current control
<2:0>	vco_bias<2:0>	W	001	vco bias current control

Reg 05h (0AAh)

Bit	Name	Type	Default value	Description
<8>	spare	W	0	Reserved
<7:6>	cf_h<1:0>	W	10	Center frequency calibration of high-frequency VCO
<5:4>	cf_mh<1:0>	W	10	Center frequency calibration of sub-high frequency VCO
<3:2>	cf_ml<1:0>	W	10	Center frequency calibration of infra-low frequency VCO
<1:0>	cf_l<1:0>	W	10	Center frequency calibration of low-frequency VCO

Reg 06h (0FFh)

Bit	Name	Type	Default value	Description
<8>	spare	W	0	Reserved
<7:6>	msb_h<1:0>	W	11	MSB calibration of high-frequency VCO segment
<5:4>	msb_mh<1:0>	W	11	MSB calibration of sub-high frequency VCO segment
<3:2>	msb_ml<1:0>	W	11	MSB calibration of infra-low frequency VCO segment
<1:0>	msb_l<1:0>	W	11	MSB calibration of low-frequency VCO segment

Product Identification Image and Pictures

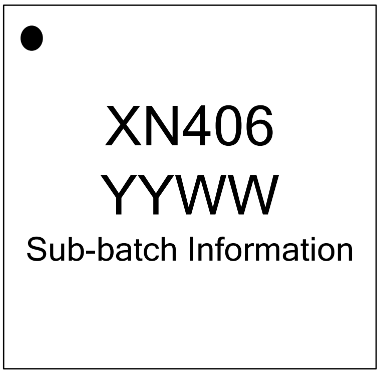
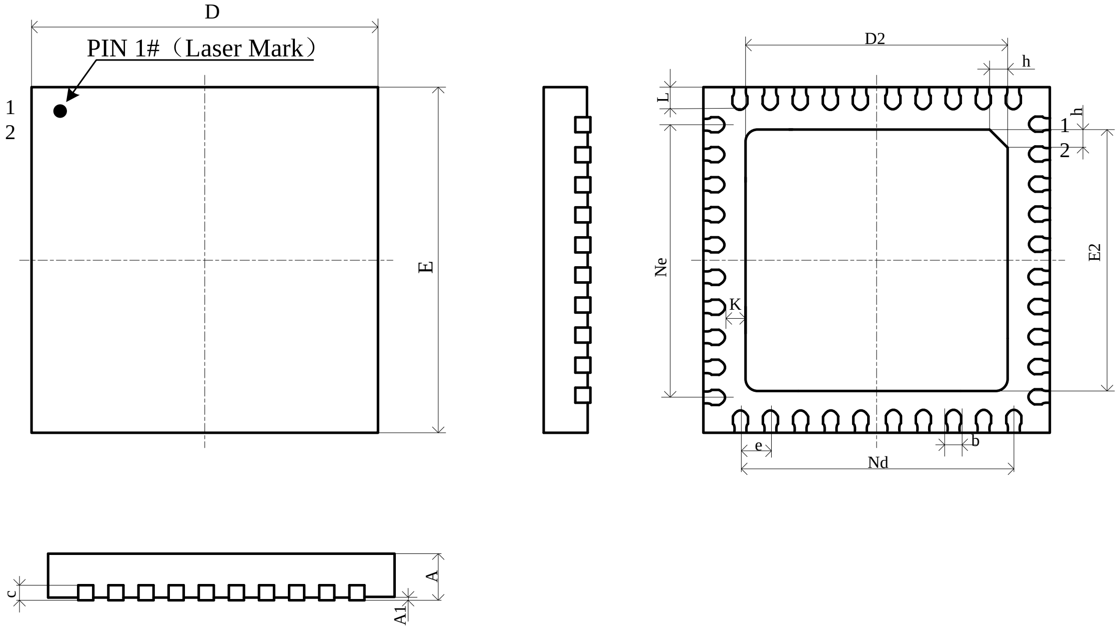


Figure 24 Product Identification

Code	Description
Upper left: ●	First pin identification

First line: XN406	Model
Second line: YYWW	Product production batch No., such as "1735" means the 35th week of the year 2017
Third line: Sub-batch information	The last 7 digits of the work order No.

Package Outline



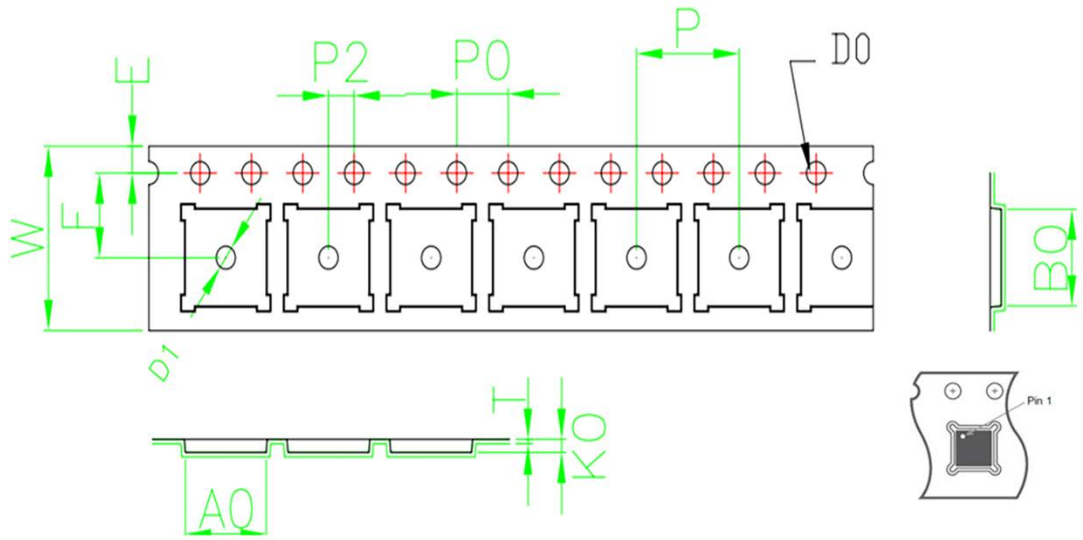
Note: 1) is the identification mark area of the leading-out terminal.

Unit: mm

Dimension Symbols	Value			Dimension Symbols	Value		
	Min.	Nominal	Max.		Min.	Nominal	Max.
A	0.70	0.75	0.80	*E2*	4.50	4.60	4.70
A1	---	0.02	0.05	*e*	---	0.50	---
b	0.20	0.25	0.30	N_d	---	4.50	---
c	---	0.203	---	N_e	---	4.50	---
D	5.90	6.00	6.10	*L*	0.35	0.40	0.45
D2	4.50	4.60	4.70	*h*	---	0.45	---
E	5.90	6.00	6.10	*K*	0.25	---	0.35

Figure 25 XN406 Package Outline

Reels of Package



W	16.00±0.30	P	8.00±0.10	A0	6.30±0.10	B0	6.30±0.10
S	0.00±0.10	P0	4.00±0.10	A1		B1	
E	1.75±0.10	P2	2.00±0.10			B2	
F	7.50±0.10	D0	ø1.50 $^{+0.10}_{-0}$	K0	1.10±0.1	K1	
T	0.30±0.05	D1	ø1.50 $^{+0.10}_{-0.10}$				

1. The cumulative error of any 10 consecutive chain holes shall not exceed ± 0.2mm.
2. The non-parallelism at the distance of 250mm in the length of the carrier tape must not exceed 1mm.
3. Material: PS, black.
4. Full size complies with the EIA-481-D.

Notes

1. Grounding: The metal base should be grounded with as many through holes as possible to reduce parasitic inductance.
2. Power supply bypass: This circuit is a hybrid RF, analog and digital circuit, the power supply pins should be filtered with capacitors of the recommended capacitance value and ensure that the capacitors are as close to the pins as possible.
3. Electrostatic discharge (ESD) damage protection: The amplifier is an ESD-sensitive device, and adequate ESD countermeasures should be taken during transmission, assembly and testing accordingly.
4. The Product Specification shall be subject to the date of release and shall be modified in due course without further notice.

Storage Condition

The moisture sensitivity level of this product is MSL 3, the product should be stored and used in accordance with the appropriate regulations of MSL 3.

Version Information

Version No.	Creation Date	Description	Page Changed
Rev 1.0	2019.12	First edition	
Rev 1.1	2020.4	Updated absolute maximum rating and added thermal	3

		resistance θ_{JA} and θ_{JC}	
		Updated the phase detector frequency range and added the minimum phase detector frequency value	4
		Updated the description of the product identification and removed the picture	18
		Updated package overall dimensions	19
Rev 1.2	2020.5	Updated the absolute maximum rating and added the thermal resistance θ_{JA}, θ_{JB}, θ_{JCbot}, Ψ_{JT} and $\Psi_{JB,}$ and modified ESD_HBM to 1000V	3
		Updated typical application circuits and added filter capacitance to the power supply	7
Rev 1.3	2020.7	Updated the absolute maximum rating and modified the junction temperature to 150°C	3
		Added frequency configuration description	9
Rev 1.4	2020.9	Added sub-batch information to the package words	19
		Updated package overall dimensions	19-20
Rev1.5	2021.4	The typical current of power supply pin was added in the "Pin Definitions"	2-3
		In "Electrical Characteristics", the minimum frequency dividing ratio of the RF divider in fractional mode was changed from 20 to 24;	4
		In "Typical Application Circuits", the schematic diagram and description of multi-chip application were added, and the filtering mode of power supply and SPI port was updated	7-8
		Added the application description of the reference input terminal in "Description"	8-9
		Added an example of the signaling process after power-on in "Description of Frequency Configuration"	11-13
		Added the "Configuration Timing Description of Power-on and Power-off SPI" in "Description"	13-14
		Added the SPI mode configuration description in "Control Interface"	14-15
		In "Register Definitions", the description part was changed to the Chinese description	16-23
		The Reg 0Fh<15> register description was added in the Register Definitions of PFD Chip	21
Rev1.6	2021.6	The configuration description was updated in the "Frequency Dividing Ratio Configuration"	10
		The Reg 00h register description was modified	16
		K value in "Package Outline" was updated from the typical value of 0.3 to a range value of 0.25 to 0.35	25
		In "Storage Conditions", it was simplified to that the product should be stored and used in accordance with the appropriate regulations of MSL 3.	25
Rev1.7	2021.7	Added information about reels of the package	25

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