FEATURES

- High accuracy, less than 0.1% error over a dynamic range of 6000:1
- High stability, less than 0.1% error in the output frequency fluctuation
- Measure the active power in the positive orientation and negative orientation, transform to fast pulse output(CF）
- Provide two current input for line and neutral current measurement
- Mesure instantaneous IRMS and VRMS over a dynamic range of 3000:1
- Provide SAG detection and Phase failure detection
- On-chip power supply detector
- On-chip anti-creep protection with the programmable threshold set
- Provide the pulse output with programmable frequency adjustment
- Provide the programmable gain adjustment and phase compensation
- Measure the power factor (PF）
- Provide a UART communication interface
- With 3.579545MHz external crystal oscillator
- On-chip voltage reference of 1.16V
- Single 5V supply, 15mW（typical）

Interralated patents are pending

DESCRIPTION

The BL6523GX is a low cost, high accuracy, high stability, electrical energy measurement IC intended to single phase, multifucion applications.

The BL6523GX incorporates three high accuracy Sigma-Delta ADC, voltage reference, power management and digital signal processing circuit using to calculates active energy, apparent energy, IRMS, VRMS etc.

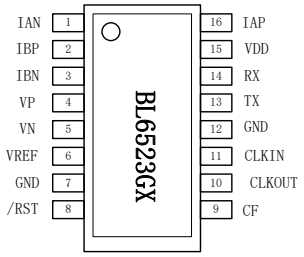
The BL6523GX have two current input for line and neutral current measurement, when these currents differ by more than the programmable Fault threshold value(RMS or WATT), the BL6523GX give the tamper detection and can enable neutral current billing,

The BL6523GX measures line voltage, current and calculates active, apparent energy, power factor, line frequency, detect sag, overvoltage, overcurrent, peak, and reverse power, zero-crossing voltage.

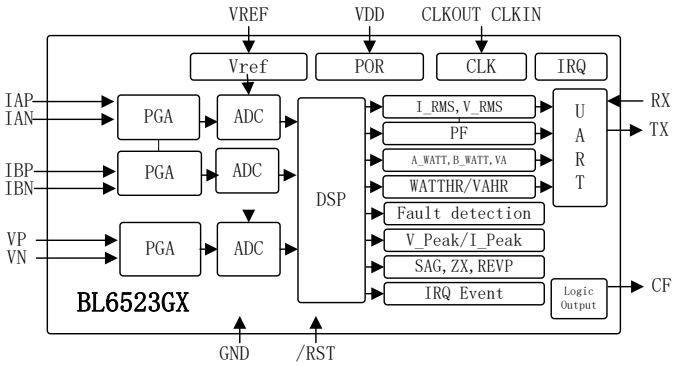
The BL6523GX provides access to on-chip meter registers via UART communication interface.

The BL6523GX provide all-digital domain offset compensation, gain adjustment, phase compensation (maximum ±1.2817° adjustable）.

BLOCK DIAGRAM



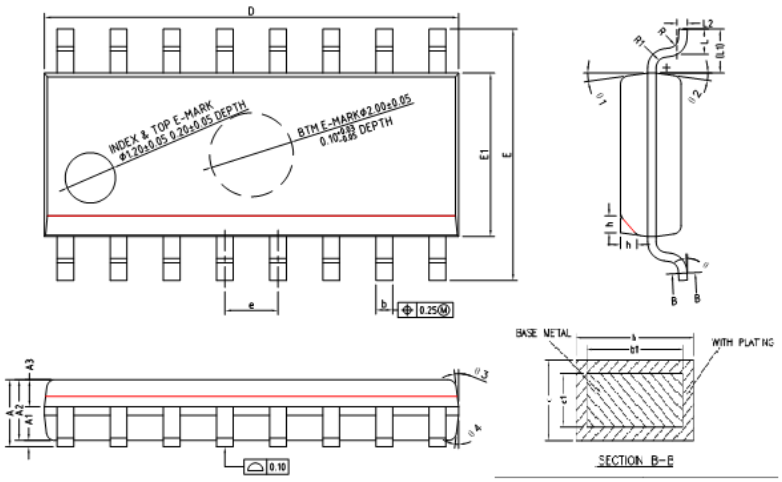
SOP16



PIN DESCRIPTIONS（SOP16）

Pin	Symbol	DESCRIPTIONS
16,1	IAP,IAN	Analog input for current channel A, These inputs are fully differential voltage inputs with a maximum signal range of ±660 mV, the PGA accociated with these inputs has a maximum gain of 16.
2,3	IBP，IBN	Analog input for current channel A, These inputs are fully differential voltage inputs with a maximum signal range of ±660 mV, the PGA accociated with these inputs has a maximum gain of 16.
4,5	VP，VN	Analog Input for Voltage Channel. These inputs are fully differential voltage inputs with a maximum signal range of ±660 mV, the PGA accociated with these inputs has a maximum gain of 16.
6	VREF	On-Chip Voltage Reference. The on-chip reference has a nominal value of 1.16V ± 8% and a typical temperature coefficient of 5ppm/℃. This pin should be decoupled with a 0.1uF ceramic capacitor. An external reference source may also be connected at this pin.
7	GND	Ground Reference.
8	/RST	Reset Pin. Logic low on this pin will hold the ADCS and digital circuitry in a reset condition and clear internal registers.
9	CF	Calibration Frequency. The CF logic output gives instantaneous real power information. This output is intended to use for calibration purposes. The full-scale output frequency can be scaled by the value of WA_CFDIV register. When the power is low, the pulse width is equal to 90ms. When the power is high and the output period less than 180ms, the pulse width equals to half of the output period.
10	CLKOUT	A crystal can be connected across this pin and Pin11 as described above to provide a clock source.
11	CLKIN	Clock Input for BL6523GX. An external clock can be provided at this logic input, Alterrnatively, a crystal (3.579545MHz) can be connected across this pin and pin10 to provide a clock source.
12	GND	Ground Reference.
13	TX	Data output for UART interface.
14	RX	Data input for UART interface.
15	VDD	Power Supply（+5V）,provides the supply voltage for BL6523GX. It should be maintained at +4.75V~+5.25V for specified operation

◆ Package Dimensions(SOP-16)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.75
A1	0.10	0.15	0.25
A2	1.35	1.45	1.55
A3	0.55	0.65	0.75
b	0.36	–	0.51
b1	0.35	0.40	0.45
c	0.18	–	0.25
c1	0.17	0.20	0.23
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.22	1.27	1.32
L	0.45	0.60	0.80
L1		1.04REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°

◆ ABSOLUTE MAXIMUM RATIONS

（T = 25 ℃）

Parameter	Symbol	Value	单位
Power Voltage AVDD、DVDD	AVDD、DVDD	-0.3 ~ +7	V
Analog Input Voltage to AGND	IAP、IBP、VP	-6 ~ +6	V
Digital Input Voltage to DGND	RX	-0.3 ~ VDD+0.3	V
Digital Output Voltage to DGND	CF, TX	-0.3 ~ VDD+0.3	V
Operating Temperature Range	Topr	-40 ~ +85	℃
Storage Temperature Range	Tstr	-55 ~ +150	℃
Power Dissipation（SOP-16）	P	80	mW

◆ Electronic Characteristic Patameter

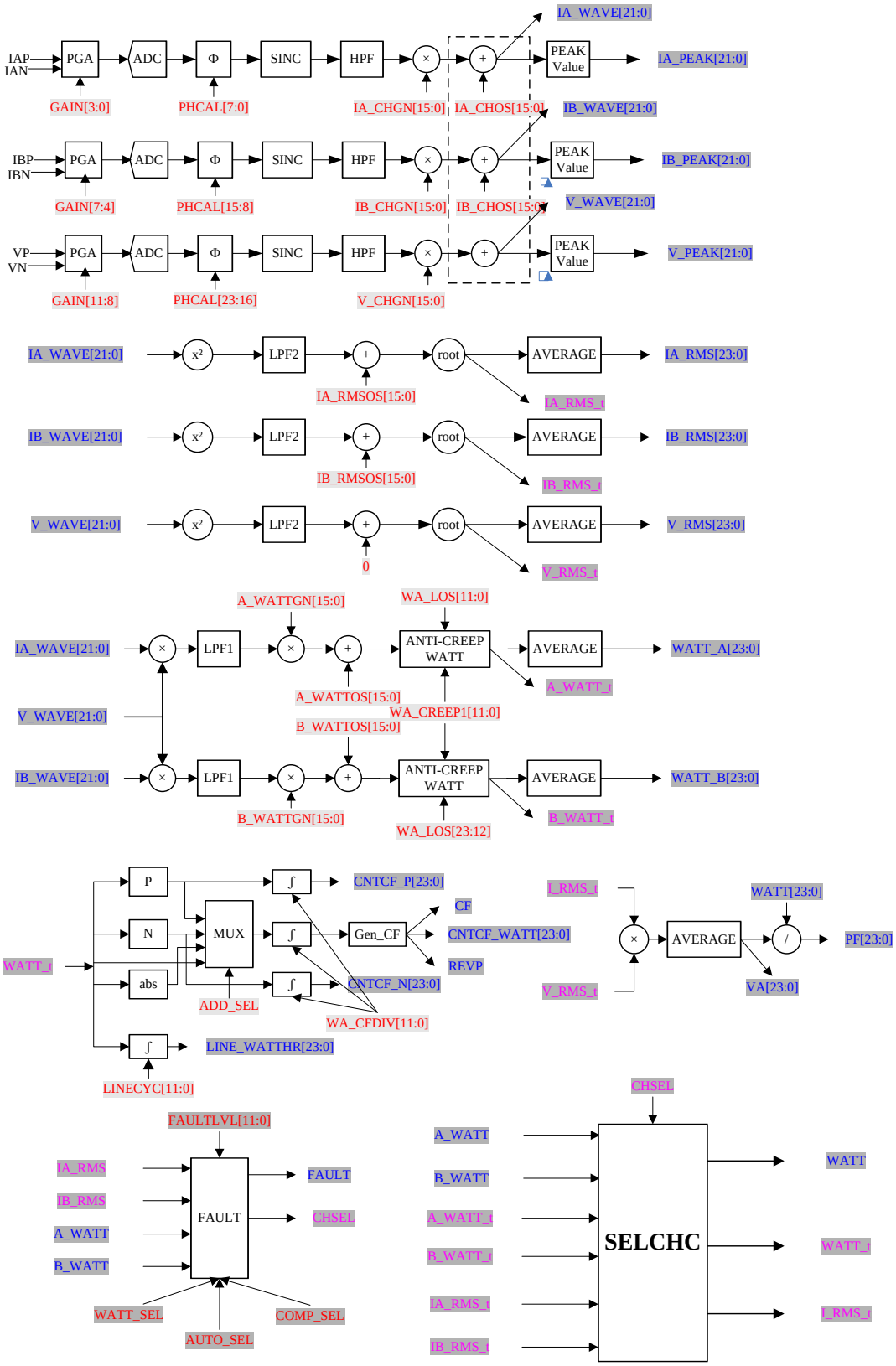
（VDD = 5V, GND＝0V, CLKIN=3.58MHz, T=25℃）

Parameter	Symbol	Test Condition	Measure Pin	Min Value	Typical Value	Max Value	Unit
Measure Error on Active Power	$WATT_{err}$	Over a dynamic range 6000:1	CF		0.1	0.3	%
Phase error when PF=0.8 Capacitive	PF08err	Current lead 37° （PF=0.8）				0.5	%
Phase error when PF=0.5Inductive	PF05err	Current lags 60° （PF=0.5）				0.5	%
AC PSRR	ACPSRR	IP/N=100mV			0.01		%
DC PSRR	DCPSRR	VP/N=100mV			0.1		%
Vrms measurement Error	VRMSerr	3000:1 input DR			0.3		%

Irms measurement Error	IRMSerr	3000:1 input DR			0.3		%
Maximum Input voltage						±660	mV
Input Impedance				370			kΩ
Input Signal Bandwidth		（-3dB）			14		kHz
Gain Error		External 1.2V reference		-4		+4	%
Gain Error match		External 1.2V reference		-1.5		+1.5	%
On-chip reference	Vref		VREF		1.16		V
Reference Error	Vreferr					±93	mV
Temperature Coefficient	TempCoef				5	15	ppm/℃
Input High Voltage		VDD=5V±5%		2.6			V
Input Low Voltage		VDD=5V±5%				0.8	V
Output High Voltage		VDD=5V±5%		4			V
Output Low Voltage		VDD=5V±5%				1	V
Power Supply	VDD			4.75		5.25	V
IDD	IDD	VDD=5.25V			3		mA

◆ THEORY OF OPERATION

System Block



◆ **Principle of Energy Measurement**

In energy measure, the power information varying with time is calculated by a direct multiplication of the voltage signal and the current signal. Assume that the current signal and the voltage signal are cosine functions, V,I are the peak values of the voltage signal and the current signal; the phase difference between the current signal and the voltage signal is expressed as Φ, Then the power is given as follows:

$$p(t) = V\cos(wt) \times I\cos(wt + \Phi)$$

If Φ=0 时:

$$p(t) = \frac{VI}{2}(1 + \cos(2wt))$$

If Φ≠0 时:

$$p(t) = V\cos(wt) \times I\cos(wt + \Phi)$$
$$= V\cos(wt) \times [I\cos(wt)\cos(\Phi) + \sin(wt)\sin(\Phi)]$$
$$= \frac{VI}{2}(1 + \cos(2wt))\cos(\Phi) + VI\cos(wt)\sin(wt)\sin(\Phi)$$
$$= \frac{VI}{2}(1 + \cos(2wt))\cos(\Phi) + \frac{VI}{2}\sin(2wt)\sin(\Phi)$$

p (t) is called as the instantaneous power signal. The ideal p(t) consists of the DC component and AC component whose frequency is 2ω. The DC component is called as the average active power.

The current signal and voltage signal is converted to digital signals by high-precsion ADCS, then through the drop sampling filter (SINC4), high-pass filter (HPF) filter out the high frequency noise and DC gain, get the required current and voltage sampling data.

Current sampling data multiplied by voltage sampling data gets instantaneous active power, then through the low pass filter (LPF), output average active power.

Current sampling data and voltage sampling data processed by square circuit, low-pass filter (LPF1), square root circuit, get the current RMS and voltage RMS.

Active power through a certain time integral, get active energy.

◆ **Front-end gain adjustment**

Every analog channel has a programmable gain amplifier (PGA), gain selection is achieved by the gain register (GAIN), the default value of the gain register (GAIN) is 000H.

Every 4-bit of the gain register used to select the current channel or voltage channel PGA. Gain[3:0] used to select Current A channel PGA,Gain[7:4] used to select Current B channel PGA, Gain[11:8] used to select Voltage channel PGA.

For example Gain [3:0]:

0000/0111=1x
0001=2x
0010=4x
0011=8x
0100=16x
0101=16x
0110=16x

◆ **Phase compensation**

BL6523GX provides the method of small phase error digital calibration. It will be a small time delay or advance into signal processing circuit in order to compensate for small phase error. Because this compensation should be promptly, so this method applies only to 0.1°~0.5° range of small phase error.

Phase calibration register (PHCAL) is a binary 24-bit register, corresponding to the compensation current A channel, current B channel and voltage channel phase. The default value is 000000H.

PHCAL [23:16] for Voltage channel;

PHCAL [15:8] for Current channel B;

PHCAL [7:0] for Current channel A;

Bit[7]/Bit[15]/Bit[23] is enable bit, when Bit[7] /Bit[15]/Bit[23] ＝ 0,disable Phase compensation; Bit[7]＝1,enable Phase compensation. Bit[6:0]/Bit[14:8]/Bit[22:16] used to adjust the delay time，0.5587us/1LSB. With a line frequency of 50Hz, the resolution is 0.0101°, The adjustable range is 0°~1.2827°.

◆ **Input channel offset calibration**

BL6523GX contains the input channel offset calibration registers (IA_CHOS, IB_CHOS), these registers are in 16-bit complement format, and the default value is 0000H. The offset may result from the analog input and the analog-digital conversion circuit itself.

◆ **Active power offset calibration**

BL6523GX contains the active power offset calibration (A_WATTOS, B_WATTOS). Both registers are in 16-bit complement format, the default value is 0000H. The offset can exist in the power calculations due to crosstalk between channels on the PCB and in the BL6523GX. The active power offset calibration allows these offsets to be removed to increase the accuracy of the measurement at low input power levels.

$$ActivePower = ActivePower_0 + X\_\text{WATTOS}$$

◆ **Active power gain adjustment**

The gain registers (A_WATTGN, B_WATTGN) are used to adjust the active power measurement range. Both registers are in 16-bit complement format, the default value is 0000H. The following formula shows how to adjust the output active power:

$$Output\ \ ActivePower = Active\ Power \times (1 + \frac{X\_WATTWG}{2^{16}})$$

The minimum value that can be write to the X_WATTGN register is 8001H(HEX), which represents a gain adjustmen of -50%. The maximum value that can be write to the X_WATTGN register is 7FFFH (HEX), which represents a gain adjustmen of +50%.

Similar gain calibration regisets are available for current channel A, current channel B and voltage channel (IA_CHGN, IB_CHGN, V_CHGN).

◆ **No-load threshold of active power**

BL6523GX contains two no-load detection features that eliminate meter creep. BL6523GX can set the no-load threshold on the active power (WA_CREEP), this register is in 24-bit unsign

magnitude format. The low 12-bit(WA_CREEP_L) is used to set the active power threshold value, When the absolute value of the input power signal is less than this threshold, the output active power is set to zero. This can make the active power register to 0 in no-load conditions, even a small noise signal input.

$$WATT = \begin{cases} 0 & , \ |WATT| < WA\_CREEP\_L \\ WATT, & |WATT| >= WA\_CREEP\_L \end{cases}$$

The high 12-bit of WA_CREEP register (WA_CREEP_H) is used to set the active power timer threshold value. The default value is 0xFFF. There have an internal TIME_CREEP register in BL6523GX, when detect the CF pulse output, the TIME_CREEP register is set to the value of WA_CREEP_H. If not detected the CF pulse output, the TIME_CREEP register value decrease. If the TIME_CREEP register decrease to 0, there is still no CF signal output, the BL6523GX produce a reset signal used to reset the internal energy accumulated register of CF pulse and reload the value of WA_CREEP_H to the TIME_CREEP register. The resolution of the WA_CREEP_H is 4.68s / LSB, so the maxium timing anti-creep time is about 5h19m.

MODE [6]=1 enable timing anti-creep function.

MODE [6]=0 disable timing anti-creep function.

- **Active power compensation of small signal**

BL6523GX contains a small active power signal compensation register (WA_LOS), this register is in 24-bit format. The default value is 0000H。

WA_LOS [11:0] for current channel A; 12-bit complement format

WA_LOS [23:12] for current channel B; 12-bit complement format

- **Active energy calculation**

The relationship between power and energy can be expressed as：

$$Power = \frac{dEnergy}{dt}$$

Conversely, energy is given as the integral of power.

$$Energy = \int Power \ dt$$

In BL6523GX, the active power signals are accumulated in a 53 internal registers continuously to get active energy, Active energy register WATTHR [23:0] take out this internal register[52:29] as active energy output. This discrete time accumulation is equivalent to integration in continuous time.

$$E = \int p(t)dt = Lim_{T\to 0}\{\sum_{n=0}^{\infty} P(nT)\times T\}$$

Where:

n is the discrete time-sample number; T is the sampling period; the sampling period of BL6523GX is 1.1us.

The BL6523GX include line cycle energy register (LINE_WATTHR). The number of cycles is writen to the LINECYC register, the LSB of the LINECYC register is 20mS. At the end of a

line cycle accumulation cycle, the LINE_WATTHR regiseter is updated. The LINE_WATTHR register hold its current value until the end of the next line cycle period, when the content is replaced with the new reading. If a new value is written to the LINECYC register midway through a line cycle accumulation, the new value is not internally loaded until the end of a line cycle period.

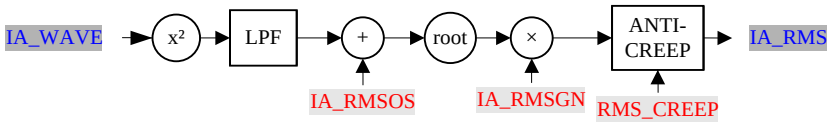
◆ **Frequency output**

The BL6523GX provides an energy-to-frequency conversion for calibration purpose. After initial calibration at manufacturing, the manufacturer or end customer is often required to verify the meter accuracy. One convenient way to do this is to provide an output frequency that is proportional to the active power. This output frequency provides a simple sigle-wire interface that can be optically isolated to interface to external calibration equipment.

BL6523GX includes a programmable calibration frequency output PIN (CF). The digital-to-frequency converter is used to generate the pulse output. The pulse output (CF) stay high for 90ms if the pulse period is longer than 180ms. If the pulse period is shorter than 180ms, the duty cycle of the pulse output is 50%. The maximum output frequency with ac inputs at full scale and with WA_CFDIV=010H is approximately 0.5 kHz.

The BL6523GX can set the CF frequency through the WA_CF_DIV register. The default value of the WA_CFDIV register is 001H (HEX). When set WA_CFDIV[x]=1, the CF frequency is $2^{(x-4)}*CF_{WA\_CFDIV=010H}$.

◆ **Root mean square measurement**



The rms is expressed mathematically as:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2(t)dt}$$

For time-sampled signals:

$$V_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} V^2(i)}$$

◆ **rms offset calibration**

BL6523GX contains the rms offset calibration (IA_RMSOS, IB_RMSOS and V_RMSOS). These registers are in 16-bit complement format, the default value is 0000H. The offset can exist in the rms calculations due to input noise that is intergrated in the dc component of square calculation. The rms offset calibration allows these offsets to be removed to increase the accuracy of the measurement at low input power levels.

$$I_{ARMS} = \sqrt{I_{ARMS0}^2 + IX\_RMSOS \times 4096 * 1.863}$$

◆ **rms gain calibration**

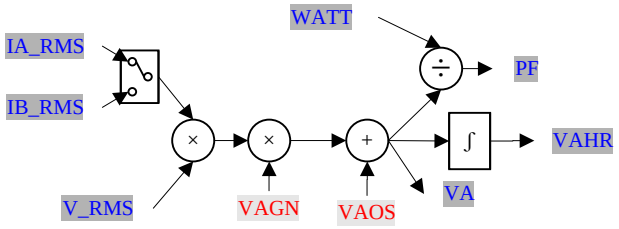
The gain registers (IA_RMSGN, IB_RMSGN and V_RMSGN) are used to adjust the rms

measurement range. Both registers are in 16-bit complement format, the default value is 0000H. The following formula shows how to adjust the rms:

$$Output\ \ rms = rms \times (1 + \frac{X\_RMSGN}{2^{16}})$$

The minimum value that can be write to the X_RMSGN register is 8001H(HEX), which represents a gain adjustment of -50%. The maximum value that can be write to the X_RMSGN register is 7FFFH (HEX), which represents a gain adjustment of +50%.

- **Apparent Power and Apparent Energy Calculation**



In BL6523GX, the apparent power is defined as the product of V_RMS and IX_RMS.

VA＝IX_RMS×V_RMS

The apparent energy is given as the intergral of the apparent power. The apparent power signals are accumulated in an internal 49-bit register, apparent energy register VAHR [23:0] take out this internal register [48:25] as apparent energy output.

- **Power Factor**

PF＝ (WATT/VA)

PF register is in 24-bit sign magnitude format. Power factor =(sign bit)*((PF[22]×2^－1）＋（PF[21]×2^－2）＋。。。), the register value of 0x7FFFFF(HEX) corresponds to a power factor value of 1, the register value of 0x800000(HEX) corresponds to a power factor of -1, the register value of 0x400000(HEX) corresponds to a power factor of 0.5.

Operation Mode Select

- **Metering channel selection**

The default metering channel of BL6523GX is channel A. the MODE [0] of MODE register is used to select the metering channel.

MODE[0]=0, the metering channel is channel A;

MODE[0]=1, the metering channel is channel B;

MODE[1]=0; disable auto channel select;

MODE[1]=1; enable auto channel select; when the chip detect the imbalance of two current channel, the chip select the bigger current channel as the metering channel.

- **High-pass filter selection**

In the analog-digital conversion circuit, the current and voltage channels have high-pass filters to eliminate the DC offset. The MODE [4:2] of MODE register is used to select high-pass filter.

MODE [2] =0, enable the high-pass filter of current channel A;

MODE [2] =1, disable the high-pass filter of current channel A;

MODE [3] =0, enable the high-pass filter of current channel B;

MODE [3] =1, disable the high-pass filter of current channel B;
MODE [4] =0, enable the high-pass filter of voltage channel;
MODE [4] =1, disable the high-pass filter of voltage channel;

- **Energy accumulation mode selection**

The MODE[9:8] of the MODE regiset is used to select energy accumulation mode.
MODE[9:8]=00, arithmetical energy accumulation;
MODE[9:8]=01, positive-only energy accumulation;
MODE[9:8]=10, absolute energy accumulation;
MODE[9:8]=11, negative-only energy accumulation;;

- **The current imbalance judgment**

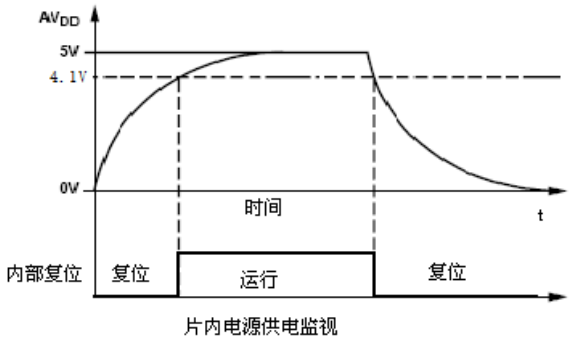
The BL6523GX contains the detection of current imbalance. MODE[11:10] of the MODE register is used to set the current rms imbalance threshold. When the Line current rms and neutral current rms difference exceeds the threshold, the BL6523GX give the FAULT indicator.

MODE[11]	MODE[10]	Threshold
0	0	12.5%(default)
0	1	6.25%
1	0	3.125%
1	1	10.1%

Electric parameters monitor

- **Power Supply Monitor**

The BL6523GX contains an on-chip power supply monitor. The power supply (VDD) is continuously monitored by the BL6523GX. if the supply is less than 4.1V±5%, the BL6523GX will be reset. This is useful to ensure correct device startup at power-up and power-down. The power supply monitor has built in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies. The power supply and decoupling for the part should be such that the ripple at AVDD does not exceed 5V±5% as specified for normal operation.



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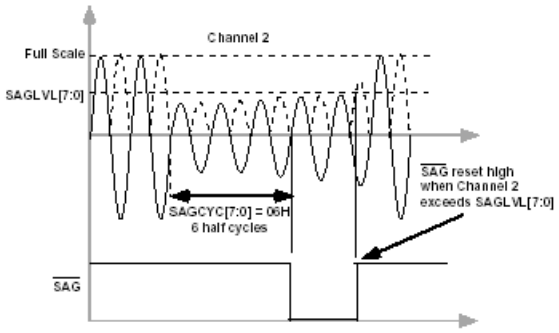
- **Zero-Crossing Detection**

The BL6523GX includes a zero-crossing detection on voltage channel. The Bit[2] of STATUS register indicate the sign of voltage wave.

- **Voltage Sag Detection**

The BL6523GX includes a sag detection features that warns the user when the absolute value

of the line voltage falls below the programmable threshold for a programmable number of half line cycles. The voltage sag feature is controlled by two registers: SAGLVL and SAGCYC. These registers control the sag voltage threshold and the sag period, respectively.



The 12-bit SAGLVL register contains the amplitude that the voltage channel must fall below before sag event occurs.The sag threshold is the number of half line cycles below which the voltage channel must remain before a sag condition occurs. Each LSB of the SAGCYC register corresponds to one half line cycle period. The default value is 0xFF(HEX). At 50Hz, the maximum sag cycle time is 2.55 seconds.

- **Peak Detection**

The BL6523GX continuously records the maximum value of the voltage channels. The three register that record the peak values on the voltage channel, respectively, are V_PEAK.

- **Peak monitor**

The BL6523GX include an overvoltage feature that detects whether the absolute value of the voltage waveform exceeds a programmable threshold. Three peak threshold register (V_PKLVL) are used to set the voltage channel peak threshold, respectively.

If the BL6523GX detects an overvoltage condition, the PKV bit of the interrupt status register is set to 1.

Interrupt

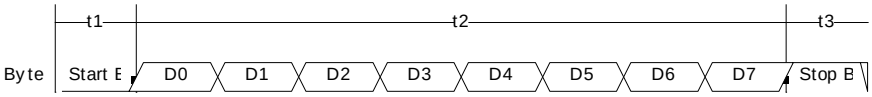
The BL6523GX uses interrupt status register and interrupt mask register to manage interrupts. When an interrupt event occurs, the corresponding bit in the STATUS register is set to 1. The status bit located in the STATUS register is set when an interrupt event occurs.

◆ UART interface

The BL6523GX provides a simple UART interface that allows all the functions of BL6523GX to be accessed using only two single-diredtion pins. This UART interface allows an isolated communication interface to be achieved using only two low cost opto-isolators.

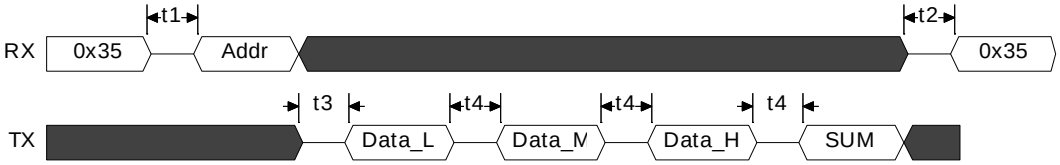
The baud rate is 4800 bps, No parity, 1 stop bit.

Byte format:



t1=t3=208uS; t2=208*8=1664uS.

Read register frame：

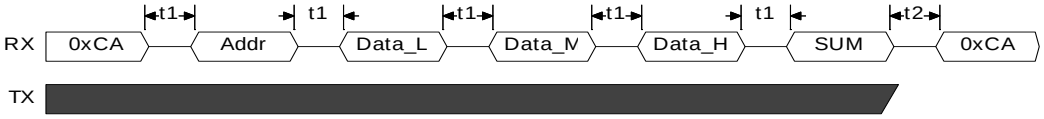


0x35: Read command byte;

Addr: BL6523GX register address;

SUM:（Addr+Data_L+Data_M+Data_H）&0xFF, then byte invert;

Write register frame:



0xCA: write command byte;

Addr: BL6523GX register address;

SUM:（Addr+Data_L+Data_M+Data_H）&0xFF, then byte invert;

		Min	Type	Max	Unit
t1	The interval between two bytes	0		20	mS
t2	The interval between two frame	0.5			uS
t3	The interval from the end of read command to the start of return data		72		uS
t4	The interval between two bytes of BL6523GX return data		116		uS

◆ Register

◆ Register list

ADDRESS	REGISTER NAME	EXTERNAL R/W	INTERNAL R/W	BIT	DEFAULT	DESCRIPTION
ELECTRIC PARAMETERS REGISTER（INTERNAL WRITE）						
01H	CF_WATTHR	R	W	24	0	CF pulse energy
04H	LINE_ WATTHR	R	W	24	0	Line cycle energy register
05H	IA_RMS	R	W	24	0	Irms register(channel A)
06H	IB_RMS	R	W	24	0	Irms register(channel B)
07H	V_RMS	R	W	24	0	Vrms
08H	PF	R	W	24	0	Power Factor
09H	FREQ	R	W	24	0	Frequency register
0AH	A_WATT	R	W	24	0	Average active power of channel A
0BH	VA	R	W	24	0	Average apparent power
0CH	COUNTER_CF	R	W	24	0	Active energy
0DH	WATTHR	R	W	24	0	Active energy of Channel B or channel A+B
0EH	COUNTER_CFP	R	W	24	0	Positive active energy
0FH	COUNTER_CFN	R	W	24	0	Negative active energy
12H	V_PEAK	R	W	24	0	Voltage Peak register
13H	B_WATT	R	W	24	0	Average active power of channel B
Calibration registers (External write，Except 3AH）						
14H	MODE	R/W	R	24	000000H	Mode regiser,
15H	GAIN	R/W	R	12	000H	Channel Gain register
16H	FAULTLVL	R/W	R	12	044H	Current imbalance shielding threshold register
17H	WA_CREEP	R/W	R	24	FFF02BH	Active power no-load threshold register
18H	WA_REVP	R/W	R	12	087H	Reverse threshold register
19H	WA_CFDIV	R/W	R	12	001H	Active power CF frequency divider

1AH	A_WATTOS	R/W	R	16	0	Active power offset correction(current channel A)
1BH	B_WATTOS	R/W	R	16	0	Active power offset correction(current B)
1CH	A_WATTGN	R/W	R	16	0	Active power gain(current channel A)
1DH	B_WATTGN	R/W	R	16	0	Active power gain(current channel B)
1EH	FREQ_SEL	R/W	R	24	6DCC 47H	Analog circuitry Frequency Control
1FH	BG_CTRL	R/W	R	22	0F5FH	Analong circuitry Control
20H	PHCAL	R/W	R	24	0	Phase calibration register
22H	BG_CTRL2	R/W	R	17	002D8 H	Analong circuitry Control
26H	IA_RMSOS	R/W	R	16	0	Current A RMS Offset Calibration register
27H	IB_RMSOS	R/W	R	16	0	Current B RMS Offset Calibration register
29H	CHKSUM_ADJ	R/W	R	12	927D2 1H	
2AH	WA_LOS	R/W	R	24	0	Active-power offset Calibration register Bit[23:12] B channel; Bit[11:0] A channel;
2EH	IA_CHGN	R/W	R	16	0	Current A channel gain adjustment register
2FH	IB_CHGN	R/W	R	16	0	Current B channel gain adjustment register
30H	V_CHGN	R/W	R	16	0	Voltage channel gain adjustment register
31H	LINECYC	R/W	R	12	000H	Line energy accumulation cycles register
32H	Reserved	R/W	R	16	FFFFH	Reversed
33H	SAGCYC	R/W	R	8	FFH	Sag period
34H	SAGLVL	R/W	R	12	0	Sag voltage level
35H	Reversed					
36H	Reserved	R/W	R	24	FFFFF	Reversed

					FH	
37H	V_PKLVL	R/W	R	12	FFFH	Voltage peak threshold
38H	AT_SEL	R/W	R	16	0	Logic output selection
39H	MASK	R/W	R	16	0	Interrupt mask register,
3AH	STATUS	R	W	16	0	Interrupt state register
Special register						
3BH	READ	R	R	24	0	Contains the data from the last read operation of SPI
3CH	WRITE	R	R	24	0	Contains the data from the last write operation of SPI
3DH	CHKSUM	R	R	24	015ABAH	Checksum。The sum of register 14H~39H(except 35H)
3EH	WRPROT	R/W	R	8	0	Write protection register. Write 55H, it means that allows write to writable register。
3FH	SOFT_NRST	R/W	/	24		Write 5A5A5AH to this register, Reset BL6523GX

Electric Parameters Registers

Waveform Register (IA_WAVE,IB_WAVE,V_WAVE)

Waveform Register of Current(IA_WAVE) Addr：01H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
Sign bit	I_WAVE22	I_WAVE21	I_WAVE20…3	I_WAVE2	I_WAVE1	I_WAVE0

Waveform Register of Current(IB_WAVE) Addr：02H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
Sign bit	I_WAVE22	I_WAVE21	I_WAVE20…3	I_WAVE2	I_WAVE1	I_WAVE0

Waveform Register of voltage(V_WAVE) Addr：03H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
Sign bit	V_WAVE22	V_WAVE21	V_WAVE20…3	V_WAVE2	V_WAVE1	V_WAVE0

Note: These registers have 24-bit complement registers, bit 23 is sign bit. The update speed of waveform register is 14 KHz.

Line Cycle Energy Register (LINE_WATTHR)

Line Cycle Active Energy Register of (LINE_WATTHR) Addr：04H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
L_AHR23	L_AHR22	L_AHR21	L_AHR20…3	L_AHR2	L_AHR1	L_AHR0

Note: This registers accumulate energy over (LINECYC+1)*0.02 second. The update speed of these registers is (LINECYC+1)*0.02 second. By using the line cycle energy accumulation mode, the energy calibration can be greatly simplified, and the time required to calibrate the meter can be significantly reduced. The accumulation time is specified in the LINECYC register.

RMS Register (IA_RMS, IB_RMS and V_RMS)

Irms register of Current(IA_RMS) Addr：05H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
RMS23	RMS22	RMS21	RMS20…3	RMS2	RMS1	RMS0

Irms register of Current(IB_RMS) Addr：06H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
RMS23	RMS22	RMS21	RMS20…3	RMS2	RMS1	RMS0

Vrms register (V_RMS) Addr：07H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
RMS23	RMS22	RMS21	RMS20…3	RMS2	RMS1	RMS0

Note: RMS value is 24-bit unsigned data. The registers updating frequency is 2.5Hz.

Power Factor Register (PF)

Power Factor Register(PF) Addr：08H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PF23	PF22	PF21	PF20…3	PF2	PF1	PF0

Note: PF23 is the sign bit. 24 bit complement register.

If PF23=0 then $PF = PF\_Reg/2^{23}$

If PF23=1 then $PF = (PF\_Reg - 2^{24})/2^{23}$

Frequency Register (FREQ)

Frequency Register(FREQ) Addr：09H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
FREQ23	FREQ22	FREQ21	FREQ20…3	FREQ2	FREQ1	FREQ0

Note: this register is the period value of the line in voltage channel.

If an 3.579545MHz crystal is used, the voltage frequency=$\frac{87.3906\times3579545}{FREQ\_Reg}$

Active Power Register (A_WATT and B_WATT)

Average active power (A_WATT) Addr：0AH			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
Sign bit	WATT22	WATT21	WATT20…3	WATT2	WATT1	WATT0

Average active power (B_WATT) Addr：13H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
Sign bit	WATT22	WATT21	WATT20…3	WATT2	WATT1	WATT0

Note: these registers are set as binary complement. The MSB is sign bit. Register updated frequency is 2.5Hz.

Assume the data in register is WATT0, then the AP for calculation is:

If WATT0<2^23, AP=WATT0;

If WATT0>=2^23, AP=WATT0-2^24;

Assume the displayed active power is P, and conversion coefficiency is Kp, then

P=AP/Kp;

Where Kp is calculated at PF=1.0, Un, Ib.

Apparent Power Register (VA)

Average apparent power register(VA) Addr：0BH			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
VA23	VA22	VA21	VA20…3	VA2	VA1	VA0

Note: The coefficient of apparent power is equal to active power coefficient.

Energy Registers（WATTHR,PWAHR,NWAHR,VAHR）

Active Energy Register(WATTHR) Addr：0CH			Type: Read		Default：000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
WTTHR23	WATTHR22	WATTHR21	WATTHR20…3	WATTHR2	WATTHR1	WATTHR0

Apparent Energy Register(VAHR) Addr：0DH			Type: Read		Default：000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
VAHR23	VAHR 22	VAHR21	VAHR20…3	VAHR2	VAHR1	VAHR0

Positive Active Energy Register(PWAHR) Addr：0EH			Type: Read		Default：000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PWAHR23	PWAHR22	PWAHR21	PWAHR20…3	PWAHR2	PWAHR1	PWAHR0

Negative Active Energy Register(NWAHR) Addr：0FH			Type: Read		Default：000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
NWAHR23	NWAHR22	NWAHR21	NWAHR20…3	NWAHR2	NWAHR1	NWAHR0

Note: these registers cannot be clear after read.

Peak Register (IA_PEAK, IB_PEAK and V_PEAK)

Current A peak register(IA_PEAK) Addr：10H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PEAK23	PEAK22	PEAK21	PEAK20…3	PEAK2	PEAK1	PEAK0

Current A peak register(IB_PEAK) Addr：11H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PEAK23	PEAK22	PEAK21	PEAK20…3	PEAK2	PEAK1	PEAK0

Voltage peak register(V_PEAK) Addr：12H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PEAK23	PEAK22	PEAK21	PEAK20…3	PEAK2	PEAK1	PEAK0

Note: the register updating frequency is 50Hz.

Calibration Registers

MODE Register (MODE)

MODE Register(MODE) Addr：14H				Type：R/W		Default：000000H	
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Bit location	Bit mnemonic	Default value	Description
0	WATT_SEL	0	The channel selection of Energy accumulation and CF output. MODE [0] =0, Current A channel. MODE [0] =1, Current B channel.
1	AUTO_SEL	0	Enable/disable Anti-tampering Mode MODE [1] =0, disable auto-switch channel. MODE [1] =1, enable auto-switch channel. When the Line and Neutral Current differ by more than the Fault_SEL threshold, the IC will auto-switch to the channel of the larger power.
2	A_HPF_SEL	0	Enable/disable the high-pass filter of current channel A MODE [2] =0, When measure AC signal input. MODE [2] =1, When measure DC signal input.
3	B_HPF_SEL	0	Enable/disable the high-pass filter of current channel B
4	V_HPF_SEL	0	Enable/disable the high-pass filter of voltage channel.
5	COMP_SEL	0	Anti-tampering MODE =0, anti-tampering mode of RMS, =1, anti-tampering mode of active power.

6	ANTICREEP_SEL	0	Anti-Creep Mode =0, anti-creep mode of active power threshold, =1, anti-creep mode of active power threshold and time-creep.
7			Reserved
8,9	CF_ADD_SEL	00	CF output mode for active power MODE[9:8]=00, absolute energy pulse output; MODE[9:8]=01, positive-only energy pulse output; MODE[9:8]=10, arithmetical energy pulse output; MODE[9:8]=11, negative-only energy pulse output;
10, 11	FAULT_SEL	00	These bits configure the L and N Line power difference threshold in anti-tampering mode Mode[11] / Mode[10] / Threshold 0 / 0 / 12.5% 0 / 1 / 6.25% 1 / 0 / 3.125% 1 / 1 / 10.16%
12 13		00	Reserved
14 15		00	Reserved
16		0	Reserved
17	CF_Disable	0	Enable/disable CF output =0, enable CF output; =1, disable CF output.
18	LOS_ADJ	0	Reserved
19	REVP_SEL	0	Reserved
20	ENG_REG_CLR	0	Reserved
21	WATTHR_SEL	0	
22 23		00	Reserved

Channel Gain Register (GAIN)

Channel Gain Register(Gain) Addr：15H	Type：R/W	Default：000H
Bit[11]~Bit[8]	Bit[7]~Bit[4]	Bit[3]~Bit[0]
Voltage channel PGA Gain	Current channel B PGA Gain	Current channel B PGA Gain

Bit	Description
11~8	Voltage PGA Gain, default value is ‘0’ Bit[11] / Bit[10] / Bit[9] / Bit[8] / PGA Gain × / 0 / 0 / 0 / 1 × / 0 / 0 / 1 / 2

	×	0	1	0	4
	×	0	1	1	8
	×	1	0	0	16
	×	1	0	1	24
	×	1	1	0	32

7~4 Current channel B PGA Gain, default value is '0'

Bit[7]	Bit[6]	Bit[5]	Bit[4]	PGA Gain
×	0	0	0	1
×	0	0	1	2
×	0	1	0	4
×	0	1	1	8
×	1	0	0	16
×	1	0	1	24
×	1	1	0	32

3~0 Current channel A PGA Gain, default value is '0'

Bit[3]	Bit[2]	Bit[1]	Bit[0]	PGA Gain
×	0	0	0	1
×	0	0	1	2
×	0	1	0	4
×	0	1	1	8
×	1	0	0	16
×	1	0	1	24
×	1	1	0	32

Imbalance Threshold Register (FAULTLVL)

Active Power Noload threshold(FAULTLVL) Addr：16H			Type：R/W		Default：004H	
Bit11	Bit10	Bit9	…	Bit2	Bit1	Bit0

When the value of the RMS/WATT is less than this threshold, the fault detection can't work.
FAULTLVL=RMS_reg/256 or FAULTLVL=WATT_reg/256.

Noload Threshold Register (WA_CREEP)

Active Power Noload threshold(WA_CREEP) Addr：17H			Type：R/W		Default：FFF02BH	
Bit23	Bit22	Bit21	…	Bit14	Bit13	Bit12
Bit11	Bit10	Bit9	…	Bit2	Bit1	Bit0

Bit[23:12] is used to set time-creep threshold. 1LSB=4.6 second.
Bit[11:0] is used to set active power noload threshold. When the absolute value of the input power signal is less than this threshold, the output active power is set to zero. This can make in no-load conditions, even a small noise signal output to the active register is 0.
One LSB in the WA_CREEP [11:0] register is equivalent to 0.366 LSBs in the WATT register.
Example: the value of WATT register is 249F0H (150000) (100%Un, 100%Ib), the starting current

of the meter is 0.4%Ib. the No-Load threshold value of active power can be set to 0.2%Ib*Un. (150000*0.2%=300), the value of WA_CREEP[11:0] is 300*0.366≈110(6EH)

Reverse Noload Threshold Register (WA_REVP)

Reverse Noload threshold(WA_REVP) Addr：18H			Type：R/W		Default：087H	
Bit11	Bit10	Bit9	…	Bit2	Bit1	Bit0

WA_REVP=WATT_reg/(32*1.3655)

When the value of X_WATT register is less than this threshold, the REVP bit of the Status register don't update and set to 0.

Note: this register only affects the status register.

CF Frequency Divider Register (WA_CFDIV)

CF output divider(WA_CFDIV) Addr：19H			Type：R/W		Default：001H	
Bit11	Bit10	Bit9	…	Bit2	Bit1	Bit0

At maximum signal level ±660mV（467mV rms）				
	Typical value			
CFDIV register(30H)	The frequency of CF（Hz）	WATT register	IA_RMS register	V_RMS register
1(001H)	1.95	6500000	5650000	5650000
2(002H)	3.91			
4(004H)	7.81			
8(008H)	15.63			
16(010H)	31.25			
32(020H)	62.50			
64(040H)	125.00			
128(080H)	250.00			
256(0100H)	500.00			

Active Power Offset Register (A_WATTOS, B_WATTOS)

Active power offset of channel A (A_WATTOS) Addr：1AH		Type：R/W	Default：0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

Active power offset of channel B (B_WATTOS) Addr：1BH		Type：R/W	Default：0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

Complement, Bit [15] is the sign bit. Power offset compensation in small power.

Assume in small power condition (5%In, PF=1.0), error of the energy meter is Err, the data of x_WATT register is WATT_Data.

If Err<0, then x_WATTOS=int ((WATT_Data*(-Err)/1.3655)*8);

If Err<0, then x_WATTOS=int((WATT_Data*(-Err)/1.3655)*8)+65536;

Active Power Gain Register (A_WATTGN, B_WATTGN)

Active power gain of channel A(A_WATTGN) Addr：1CH		Type：R/W	Default：0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

Active power gain of channel B(B_WATTGN) Addr：1DH		Type：R/W	Default：0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

Complement, Bit [15] is the sign bit.

Output WATT_Reg=Active Power $*(1+\frac{X_{WATTGN}}{2^{16}})$

Phase Calibration Registers (PHCAL_I, PHCAL_V)

PHCAL Register(PHCAL) Addr：20H				Type：R/W			Default：000000H
Enable bit	Phase compensaton of current channel A						
D7	D6	D5	D4	D3	D2	D1	D0
Enable bit	Phase compensaton of current channel B						
D15	D14	D13	D12	D11	D10	D9	D8
Enable bit	Phase compensaton of voltage channel						
D23	D22	D21	D20	D19	D18	D17	D16

Bit[7]/Bit[15]/Bit[23] is enable bit, when Bit[7]/Bit[15]/Bit[23] = 0,disable compensation; Bit[7]/Bit[15]/Bit[23]=1,enable compensation. Bit[6:0]/Bit[14:8]/Bit[22:16] used to adjust the delay time，1.1us/1LSB. With a line frequency of 50Hz, the resolution is 360°×（1/900KHz）×50Hz=0.02°, The adjustable range is 0°~2.54°.

1LSB of register may cause the accuracy Error change 0.0605%.

If Error>=0, write the adjust value to Phase compensation of current channel.

If Error<0, write the adjust Value to Phase compensation of voltage channel.

The value=int (|Err|/0.0605) +127.

Apparent power offset Register (VA_OS)

Apperant power offset (VAOS) Addr：21H		Type：R/W	Default：0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

Complement, Bit [15] is the sign bit.

VA=VA0+VAOS.

Apparent Power Gain Register (VAGN)

Apparent power gain (VAGN) Addr：22H		Type：R/W	Default：0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

Complement, Bit [15] is the sign bit.

Output VA_reg=VA0 $*(1+\frac{VAGN}{2^{16}})$

RMS Gain Register (IA_RMSGN, IB_RMSGN and V_RMSGN)

RMS gain of current A(IA_RMSGN) Addr: 23H		Type: R/W	Default: 0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

RMS gain of current B(IB_RMSGN) Addr: 24H		Type: R/W	Default: 0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

RMS gain of voltage(V_RMSGN) Addr: 25H		Type: R/W	Default: 0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

Complement, Bit [15] is the sign bit.

Output x_RMS_reg=x_RMS0∗ $(1+\frac{\text{x\_RMSGN}}{2^{16}})$

RMS Offset Registers (IA_RMSOS, IB_RMSOS, V_RMSOS)

RMS offset of current A(IA_RMSOS) Addr: 26H		Type: R/W	Default: 0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

RMS offset of current B(IB_RMSOS) Addr: 27H		Type: R/W	Default: 0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

RMS offset of voltage(V_RMSOS) Addr: 28H		Type: R/W	Default: 0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

Complement, Bit [15] is the sign bit.

$$I_{ARMS} = \sqrt{I_{ARMS\,0}{}^2 + IA\_RMSOS \times 2^{13}}$$

RMS Noload Threshold Register (RMS_CREEP)

RMS Noload threshold(RMS_CREEP) Addr: 29H		Type: R/W	Default: 000H
Bit11	Bit10～8	Bit7～4	Bit3～0

$$\text{RMS} = \begin{cases} 0 & RMS < RMS\_CREEP \times 1.3655/4 \\ \text{RMS}, & RMS >= RMS\_CREEP \times 1.3655/4 \end{cases}$$

Please refer to chapter “No-load threshold of RMS”

Small signal compensation of Active power (WA_LOS)

These two registers do not need change. Keep the default value.

Channel Offset Registers (IA_CHOS, IB_CHOS, V_CHOS)

These two registers do not need change. Keep the default value.

Calibration Gain Register (IA_CHGN, IB_CHGN, V_CHGN)

Calibration gain of current A (IA_CHGN) Addr：2EH		Type：R/W	Default：0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

Calibration gain of current B (IB_CHGN) Addr：2FH		Type：R/W	Default：0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

Calibration gain of Voltage (V_CHGN) Addr：30H		Type：R/W	Default：0000H
Bit15(sign bit)	Bit14～8	Bit7～4	Bit3～0

Complement, Bit [15] is the sign bit.

L line gain calibration is performed when PF=1.0 and the current is In.

Assume the error output of the calibration bench is Err.

If Err <0, then GN=int ($2^{16} \times \frac{-Err}{1+Err}$)

If Err>=0, then GN=int ($2^{16} + 2^{16} \times \frac{-Err}{1+Err}$)

The Err can be calibrated when the Err range is -33.3%~+99.9%

The GN value can be set to 2EH or 30H register.

Line Energy Accumulation Cycle Register (LINECYC)

Line Energy Cycle(LINECY) Addr：31H			Type：R/W		Default：000H	
Bit11	Bit10	Bit9	…	Bit2	Bit1	Bit0

Note: set the LINE_WATTHR, LINE_VARHR.LINE_VAHR update period. The LSB of the LINECYC register is 0.02S. At the end of a line cycle accumulation cycle, the LINE_WATTHR register is updated. The LINE_WATTHR register hold its current value until the end of the next line cycle period, when the content is replaced with the new reading. If a new value is written to the LINECYC register midway through a line cycle accumulation, the new value is not internally loaded until the end of a line cycle period.

Zero-Crossing TimeOut Register (ZXTOUT)

Zero-Crossing TimeOut(ZXTOUT) Addr：32H	Type：R/W	Default：FFFFH

Bit15～12	Bit11～8	Bit7～4	Bit3～0

70.5uS/LSB.

Please refer to chapter “Electric parameters monitor”

SAG Detection Register (SAGCYC, SAGLVL)

(SAGCYC) Addr：33H				Type：R/W		Default：FFH	
D7	D6	D5	D4	D3	D2	D1	D0

10mS/LSB.

(SAGLVL) Addr：34H		Type：R/W	Default：FFH
Bit11	Bit10～8	Bit7～4	Bit3～0

The value compare with V_RMS [23:12].

Please refer to chapter “Electric parameters monitor”

Peak Detection Register (I_PKLVL, V_PKLVL)

Current peak level(I_PKLVL) Addr：36H		Type：R/W	Default：000000H
Bit23～Bit16	Bit15～12	Bit11～4	Bit3～0
Reserved		Current A/B peak level	

Voltage peak level(V_PKLVL) Addr：37H		Type：R/W	Default：000H
Bit11	Bit10～8	Bit7～4	Bit3～0

Please refer to chapter “Electric parameters monitor”

Logic output control register(ATT_SEL)

This register does not need change. Keep the default value.

Interrupt Mask Register(MASK)

Interrupt Mask Register(MASK) Addr：39H				Type:R/W	Default:0000H
D15	D14	D13	D12…D2	D1	D0

This register does not need change. Keep the default value.

Interrupt Status Register

Interrupt Status Register(STATUS) Addr：3AH			Type:Read	Default:0000H
D15	D14	D13	D12…D2	D1	D0

BIT LOCATION	INTERRUPT FLAG	DEFAULT	DESCRIPTION
0	SAG	0	Indicates that an interrupt was caused by a Sag event
1	ZXTO	0	Indicates that zero crossing has been missing on the voltage channel for the length of time specified

			in the ZXTOUT register
2	ZX	0	Voltage channel zero crossing
3	PKIA	0	Current channel A peak has exceeded I_PKLVL
4	PKIB	0	Current channel B peak has exceeded I_PKLVL
5	PKV	0	Voltage peak has exceeded V_PKILVL
6	REVP	0	Indicates the active power has gone from positive to negative(instantaneous power)
7	APEHF	0	Indicates that an interrupt was caused because WATTHR register is more than half full
8	VAPEHF	0	Indicates that an interrupt was caused because WAHR register is more than half full
9	FAULT	0	Indicates the Line and Neutral signal imbalance
10	CHSEL	0	Indicates the channel of CF output
11	VREF_LOW	0	Indicates that the reference voltage is lower than 2V
12~15	Reversed		Reversed

Read/Write Register (Read/Write)

Read Register(READ) Addr：3BH				Type：R	默认值：000000H	
Bit23	Bit22	Bit21	…	Bit2	Bit1	Bit0

Write Register(WRITE) Addr：3CH				Type：R	默认值：000000H	
Bit23	Bit22	Bit21	…	Bit2	Bit1	Bit0

Note: these register store the data that is just read or written through the UART interface.

Checksum Register (CHKSUM)

Checksum Register(CHKSUM) Addr：3DH				Type：R	默认值：015A4AH	
Bit23	Bit22	Bit21	…	Bit2	Bit1	Bit0

Note: this register is the sum of register 14H~39H Value (except 35H). If the value of these register changed, the CHKSUM will be written the new value automatically.

Write Protection Register (WRPROT)

Write Protection Register(WRPROT) Addr：3EH				Type：R	默认值：00H	
Bit7	Bit6	Bit5	…	Bit2	Bit1	Bit0

Note: when the calibration registers of BL6523GX can be written after only the 55H is written to this register.

SOFT_NRST Register (SOFT_NRST)

Software Reset Register(SOFT_NRST) Addr：3FH			Type：W		默认值：000000H	
Bit23	Bit22	Bit21	…	Bit2	Bit1	Bit0

Note: Software Reset register. When enable write operation (WRPROT=55H), the BL6528 resets if only 5A5A5AH is written to this register.