NSi8220/NSi8221/NSi8222:
High Reliability Dual-Channel Digital Isolators

Datasheet (EN) 1.1

Product Overview

The NSi822x devices are high reliability dual-channel digital isolator. The NSi822x device is safety certified by UL1577 support several insulation withstand voltages (3.75kVrms, 5kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi822x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The NSi822x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi822x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use. AEC-Q100 (Grade 1) option is provided for all devices.

Key Features

- Up to 5000V_{rms} Insulation voltage
- Date rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- All devices are AEC-Q100 qualified
- High CMTI: 200kV/us
- Chip level ESD: HBM: ±8kV
- Robust EMC Reinforced Dual-Channel Digital Isolators for SOW8 wide body and SOW16 wide body
- Default output high level or low level option
- Isolation surge voltage: >10kV
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  - SOP8 narrow body
  - SOW8 wide body
  - SOW16 wide body

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Device Information

Part Number	*Package*	*Body Size*
NSI822xNx-DSPR	SOP8	4.90mm × 3.90mm
NSI822xWx-DSWVR	SOW8	5.85mm × 7.50mm
NSI822xWx-DSWR	SOW16	10.30mm × 7.50mm

Functional Block Diagrams

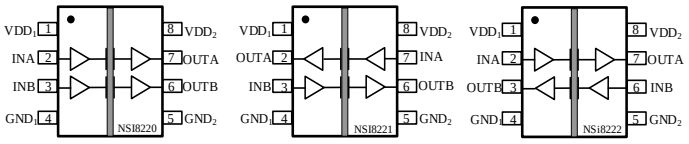

Figure 1. NSi822xN Block Diagram

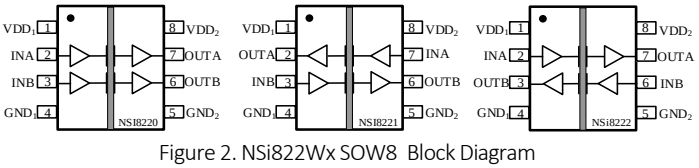

Figure 2. NSi822Wx SOW8 Block Diagram

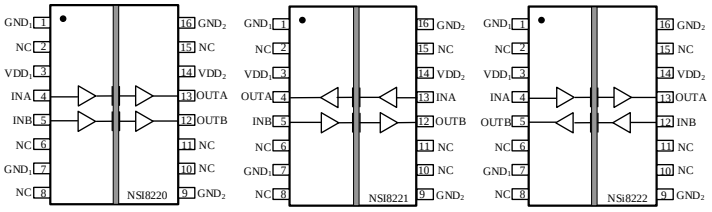

Figure 3. NSi822Wx SOW16 Block Diagram

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1. Pin Configuration and Functions

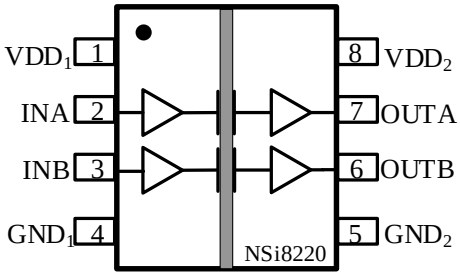

Figure 1.1 NSi8220N Package

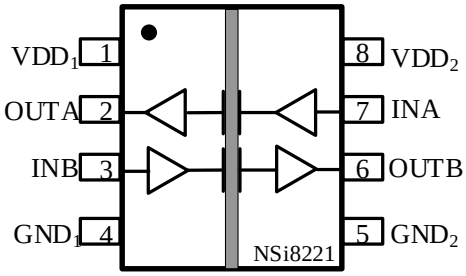

Figure 1.2 NSi8221N Package

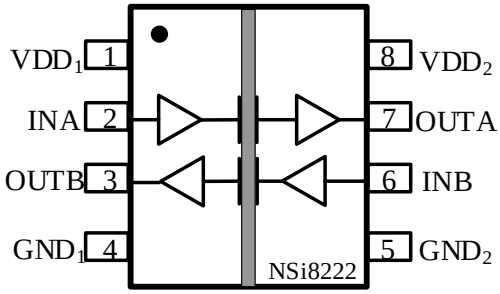

Figure 1.3 NSi8222N Package

Table1.1 NSi8220N/ NSi8221N/ NSi8222N Pin Configuration and Description

NSi8220N PIN NO.	*NSi8221N PIN NO.*	*NSi8222N PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	1	VDD1	Power Supply for Isolator Side 1
2	7	2	INA	Logic Input A
3	3	6	INB	Logic Input B
4	4	4	GND1	Ground 1, the ground reference for Isolator Side 1
5	5	5	GND2	Ground 2, the ground reference for Isolator Side 2
6	6	3	OUTB	Logic Output B
7	2	7	OUTA	Logic Output A
8	8	8	VDD2	Power Supply for Isolator Side 2

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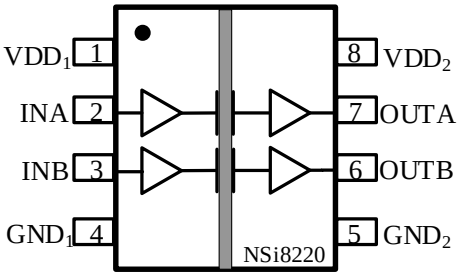

Figure 1.4 NSi8220Wx SOW8 Package

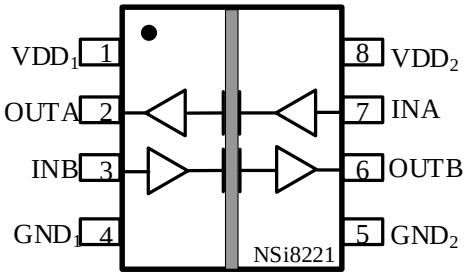

Figure 1.5 NSi8221Wx SOW8 Package

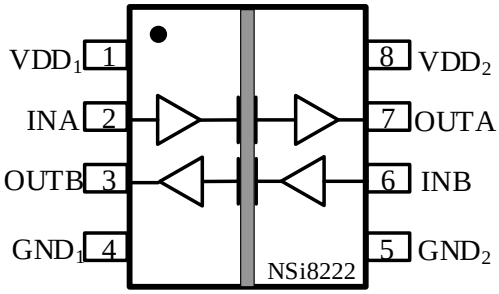

Figure 1.6 NSi8222Wx SOW8 Package

Table1.2 NSi8220Wx/ NSi8221Wx/ NSi8222Wx SOW Pin Configuration and Description

NSi8220W PIN NO.	*NSi8221W PIN NO.*	*NSi8222W PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	1	VDD1	Power Supply for Isolator Side 1
2	7	2	INA	Logic Input A
3	3	6	INB	Logic Input B
4	4	4	GND1	Ground 1, the ground reference for Isolator Side 1
5	5	5	GND2	Ground 2, the ground reference for Isolator Side 2
6	6	3	OUTB	Logic Output B
7	2	7	OUTA	Logic Output A
8	8	8	VDD2	Power Supply for Isolator Side 2

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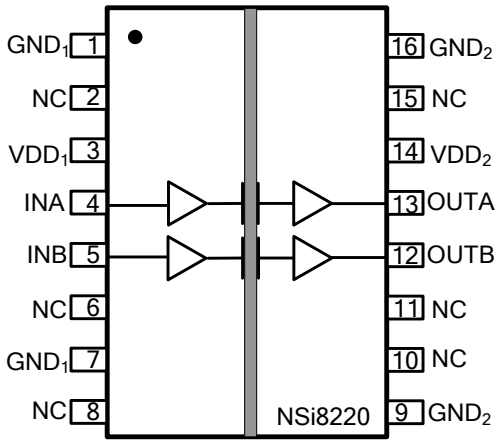

Figure 1.7 NSi8220W Package

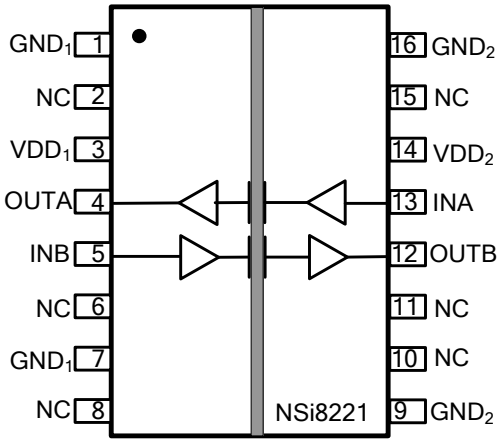

Figure 1.8 NSi8221W Package

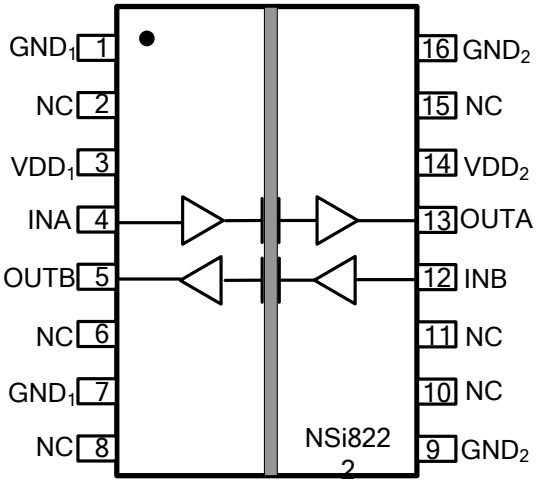

Figure 1.9 NSi8222W Package

Table 1.2 NSi8220W/ NSi8221W/ NSi8222W Pin Configuration and Description

NSi8220W PIN NO.	*NSi8221W PIN NO.*	*NSi8222W PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	1	GND1	Ground 1, the ground reference for Isolator Side 1
2	2	2	NC	No Connection.
3	3	3	VDD1	Power Supply for Isolator Side 1
4	13	4	INA	Logic Input A
5	5	12	INB	Logic Input B
6	6	6	NC	No Connection.
7	7	7	GND1	Ground 1, the ground reference for Isolator Side 1
8	8	8	NC	No Connection.

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9	9	9	GND2	Ground 2, the ground reference for Isolator Side 2
10	10	10	NC	No Connection.
11	11	11	NC	No Connection.
12	12	5	OUTB	Logic Output A
13	4	13	OUTA	Logic Output B
14	14	14	VDD2	Power Supply for Isolator Side 2
15	15	15	NC	No Connection.
16	16	16	GND2	Ground 2, the ground reference for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB	-0.4		VDD+0.4[1]	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	V_{OUTA}, V_{OUTB}	-0.4		VDD+0.4[1]	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	VINA, VINB, V_{OUTA}, V_{OUTB}	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Common-Mode Transients	CMTI			±200	kV/us	
Output current	Io	-15		15	mA	
Operating Temperature	Topr	-40		125	℃	
Junction temperature	Tj	-40		150	℃	
Storage Temperature	Tstg	-40		150	℃	
Electrostatic discharge	HBM			±8000	V	
	CDM			±2000	V	

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3. Recommended Operating Conditions

Parameters	*Symbol*	*min*	*typ*	*max*	*unit*
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	Topr	-40		125	℃
High Level Input Voltage	VIH	2			V
Low Level Input Voltage	VIL			0.8	V
Data rate	DR			150	Mbps

4. Thermal Characteristics

Parameters	*Symbol*	*SOW16*	*SOW8*	*SOP8*	*Unit*
IC Junction-to-Air Thermal Resistance	θ_{JA}	86.5	84.3	137.7	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	49.6	36.3	54.9	°C/W
Junction-to-board thermal resistance	θ_{JB}	49.7	47.0	71.7	°C/W

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5. SPECIFICATIONS

5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power on Reset	VDD_{POR}		2.2		V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
Input Threshold	V_{IT}		1.6		V	Input Threshold at rising edge
	V_{IT_HYS}		0.4		V	Input Threshold Hysteresis
High Level Input Voltage	V_{IH}	2			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Output Voltage	V_{OH}	VDD-0.4			V	I_{OH} ≤ 4mA
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} ≤ 4mA
Output Impedance	R_{out}		50		ohm	
Input Pull high or low Current	I_{pull}		8	15	uA	
Start Up Time after POR	trbs		10		usec	
Common Mode Transient Immunity	CMTI	±150		±200	kV/us	See Figure 5.8

5.2. Supply Current Characteristics – 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSi8220**					
	I_{DD1}(Q0)		0.59	0.89	mA	All Input 0V for NSi8220x0 Or All Input at supply for NSi8220x1
	I_{DD2}(Q0)		1.29	1.94	mA	
	I_{DD1}(Q1)		2.80	4.20	mA	All Input at supply for NSi8220x0 Or All Input 0V for NSi8220x1
	I_{DD2}(Q1)		1.32	1.98	mA	
	I_{DD1}(1M)		1.70	2.55	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.39	2.09	mA	
	I_{DD1}(10M)		1.78	2.67	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.13	3.20	mA	
	I_{DD1}(100M)		2.49	3.74	mA	All Input with 100Mbps,

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	I_{DD2}(100M)		9.22	13.83	mA	C_L=15pF
	NSi8221/ NSi8222					
	I_{DD1}(Q0)		0.94	1.41	mA	All Input 0V for NSi822xx0 Or All Input at supply for NSi822xx1
	I_{DD2}(Q0)		0.94	1.41	mA	
	I_{DD1}(Q1)		2.06	3.09	mA	All Input at supply for NSi822xx0 Or All Input 0V for NSi822xx1
	I_{DD2}(Q1)		2.06	3.09	mA	
	I_{DD1}(1M)		1.55	2.32	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.55	2.32	mA	
	I_{DD1}(10M)		1.96	2.93	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		1.96	2.93	mA	
	I_{DD1}(100M)		5.86	8.78	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		5.86	8.78	mA	

5.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	NSi8220					
	I_{DD1}(Q0)		0.56	0.83	mA	All Input 0V for NSi8220x0 Or All Input at supply for NSi8220x1
	I_{DD2}(Q0)		1.24	1.86	mA	
	I_{DD1}(Q1)		2.76	4.13	mA	All Input at supply for NSi8220x0 Or All Input 0V for NSi8220x1
	I_{DD2}(Q1)		1.27	1.91	mA	
	I_{DD1}(1M)		1.66	2.49	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.31	1.97	mA	
	I_{DD1}(10M)		1.71	2.57	mA	All Input with 10Mbps, C_L = 15pF
	I_{DD2}(10M)		1.80	2.70	mA	
	I_{DD1}(100M)		2.20	3.30	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		6.50	9.75	mA	
	NSi8221/ NSi8222					
	I_{DD1}(Q0)		0.90	1.35	mA	All Input 0V for NSi822xx0 Or All Input at supply for NSi822xx1
	I_{DD2}(Q0)		0.90	1.35	mA	
	I_{DD1}(Q1)		2.01	3.02	mA	All Input at supply for NSi822xx0 Or All Input 0V for NSi822xx1
	I_{DD2}(Q1)		2.01	3.02	mA	

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	I_{DD1}(1M)		1.49	2.23	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.49	2.23	mA	
	I_{DD1}(10M)		1.76	2.63	mA	All Input with 10Mbps, C_L = 15pF
	I_{DD2}(10M)		1.76	2.63	mA	
	I_{DD1}(100M)		4.35	6.53	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		4.35	6.53	mA	

5.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSi8220**					
	I_{DD1}(Q0)		0.54	0.81	mA	All Input 0V for NSi8220x0 Or All Input at supply for NSi8220x1
	I_{DD2}(Q0)		1.22	1.83	mA	
	I_{DD1}(Q1)		2.73	4.10	mA	All Input at supply for NSi8220x0 Or All Input 0V for NSi8220x1
	I_{DD2}(Q1)		1.24	1.86	mA	
	I_{DD1}(1M)		1.64	2.46	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.27	1.91	mA	
	I_{DD1}(10M)		1.67	2.51	mA	All Input with 10Mbps, C_L = 15pF
	I_{DD2}(10M)		1.65	2.48	mA	
	I_{DD1}(100M)		1.98	2.97	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		5.22	7.83	mA	
	NSi8221/ NSi8222					
	I_{DD1}(Q0)		0.88	1.32	mA	All Input 0V for NSi822xx0 Or All Input at supply for NSi822xx1
	I_{DD2}(Q0)		0.88	1.32	mA	
	I_{DD1}(Q1)		1.99	2.98	mA	All Input at supply for NSi822xx0 Or All Input 0V for NSi822xx1
	I_{DD2}(Q1)		1.99	2.98	mA	
	I_{DD1}(1M)		1.46	2.18	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.46	2.18	mA	
	I_{DD1}(10M)		1.66	2.49	mA	All Input with 10Mbps, C_L = 15pF
	I_{DD2}(10M)		1.66	2.49	mA	
	I_{DD1}(100M)		3.60	5.40	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		3.60	5.40	mA	

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5.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V,** Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	6.54	15	ns	See Figure 5.7 , C_L = 15pF
	t_{PHL}	2.5	8.30	15	ns	See Figure 5.7 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 5.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.7 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.7 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

5.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V,** Ta = 25℃)

Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	8.0	15	ns	See Figure 5.7 , C_L = 15pF
	t_{PHL}	2.5	8.7	15	ns	See Figure 5.7 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 5.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.7 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.7 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

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5.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V,** Ta = 25℃)

Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	9.0	15	ns	See Figure 5.7 , C_L = 15pF
	t_{PHL}	2.5	9.3	15	ns	See Figure 5.7 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 5.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.7, C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.7, C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

5.8. Typical Performance Characteristics

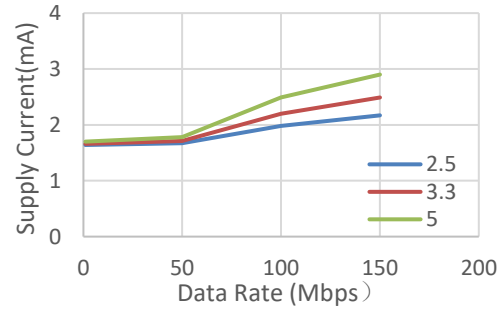

Figure 5.1 NSi8220 VDD1 Supply Current vs Data Rate

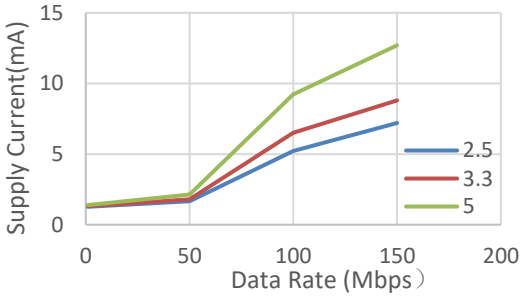

Figure 5.2 NSi8220 VDD2 Supply Current vs Data Rate

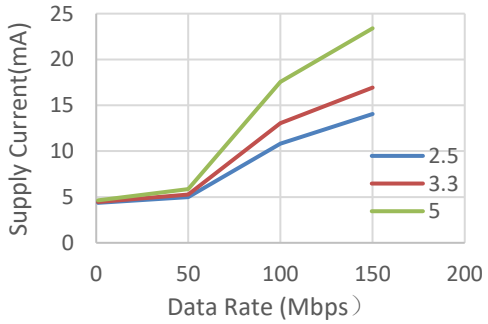

Figure 5.3 NSi8221/ NSi8222 VDD1 Supply Current vs Data Rate

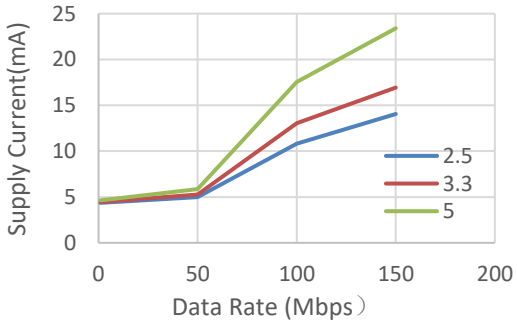

Figure 5.4 NSi8221/ NSi8222 VDD2 Supply Current vs Data Rate

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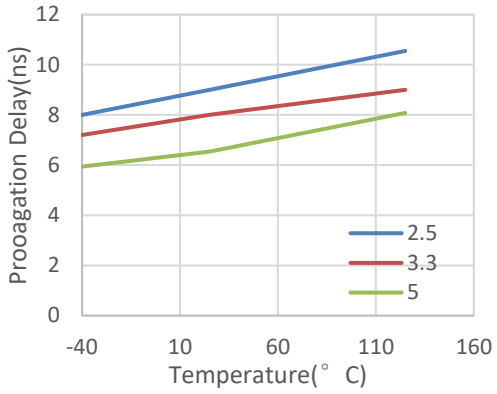

Figure 5.5 Rising Edge Propagation Delay Vs Temp

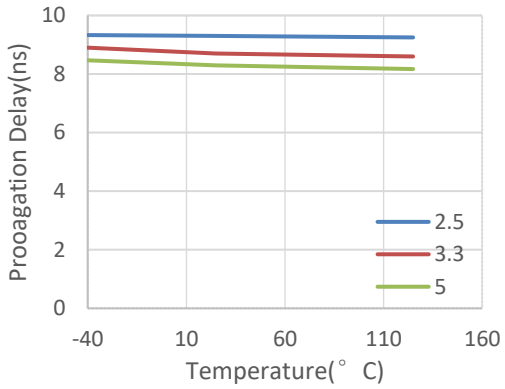

Figure 5.6 Falling Edge Propagation Delay Vs Temp

5.9. Parameter Measurement Information

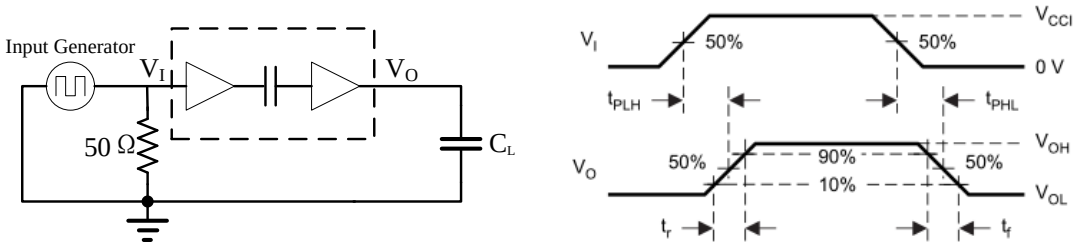

Figure 5.7 Switching Characteristics Test Circuit and Waveform

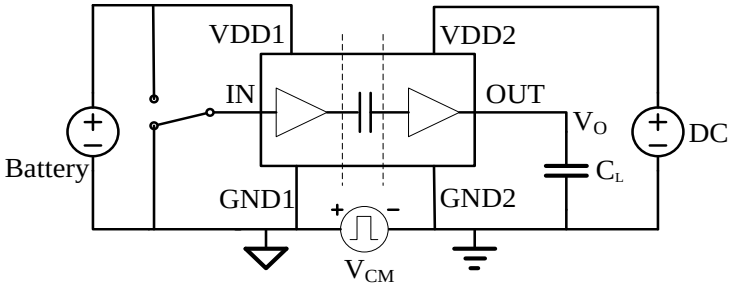

Figure 5.8 Common-Mode Transient Immunity Test Circuit

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6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*			*Unit*	*Comments*
		SOP8	*SOW_8*	*SOW-16*		
Minimum External Air Gap (Clearance)	L(I01)	4.0	8.0	8.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0	8.0	8.0	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20			um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>600			V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I				

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6.2. DIN VDE V 0884-11（VDE V 0884-11）:2017-01 Insulation Charateristics

Description	*Test Condition*	*Symbol*	*Value*			*Unit*
			SOP8	SOW8	SOIC-16	
Installation Classification per DIN VDE 0110						
For Rated Mains Voltage ≤ 150V_{rms}			Ⅰ to Ⅳ	Ⅰ to Ⅳ	Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 300V_{rms}			Ⅰ to Ⅲ	Ⅰ to Ⅳ	Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 400V_{rms}			Ⅰ to Ⅲ	Ⅰ to Ⅳ	Ⅰ to Ⅳ	
Climatic Classification			10/105/21	10/105/21	10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	2	
Maximum repetitive isolation voltage		V_{IORM}	565	2121	2121	Vpeak
Input to Output Test Voltage, Method B1	V_{IORM} × 1.5 = $V_{pd(m)}$, 100% production test, t_{ini} = t_m = 1 sec, q_{pd} < 5 pC	$V_{pd(m)}$	847	/	/	Vpeak
	V_{IORM} × 1.875 = $V_{pd(m)}$, 100% production test, t_{ini} = t_m = 1 sec, q_{pd} < 5 pC		/	3977	3977	
Input to Output Test Voltage, Method A						
After Environmental Tests Subgroup 1	V_{IORM} × 1.2=$V_{pd(m)}$, t_{ini} = 60 sec, t_m=10 sec, q_{pd} < 5 pC	$V_{pd(m)}$	678	/	/	Vpeak
	V_{IORM} × 1.6=$V_{pd(m)}$, t_{ini} = 60 sec, t_m=10 sec, q_{pd} < 5 pC		/	3394	3394	
After Input and /or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2= $V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	678	2545	2545	Vpeak
Maximum transient isolation voltage	t = 60 sec	VIOTM	5300	8000	8000	Vpeak
Maximum withstanding isolation voltage	V_{TEST}= V_{ISO}, t = 60 s (qualification); VTEST= 1.2 × VISO, t = 1 s (100%production)	VISO	3750	5000	5000	V_{RMS}
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, VTEST=VIOSM×1.3	VIOSM	5384			Vpeak
	Test method per IEC60065,1.2/50us waveform, VTEST=VIOSM×1.6			6250	6250	Vpeak

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Isolation resistance	V_{IO} =500V at T_{amb}=T_S	RIO	>10^9	>10^9	>10^9	Ω
	V_{IO} =500V at 100℃≤T_{amb}≤125℃		>10^{11}	>10^{11}	>10^{11}	Ω
Isolation capacitance	f = 1MHz	CIO	0.6	0.6	0.6	pF
Input capacitance		CI	2	2	2	pF
Total Power Dissipation at 25℃		Ps	1100	674.4	692	mW
Safety input, output, or supply current	θJA = 137.7 °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C	Is	165			mA
	θJA = 84.3 °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C			269.6		
	θJA = 86.5 °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C				262.7	mA
Case Temperature		Ts	150	150	150	℃

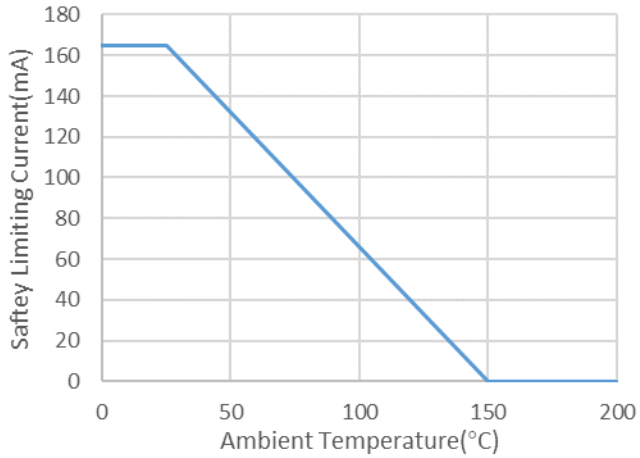

Figure 6.1 NSi822xN-DSPR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

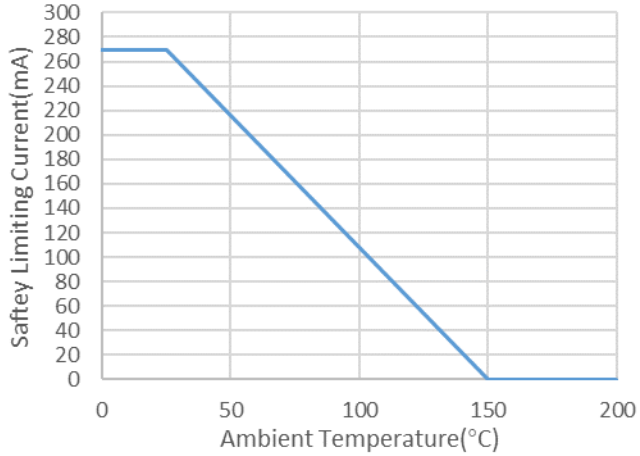

Figure 6.2 NSi822xW-DSWVR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

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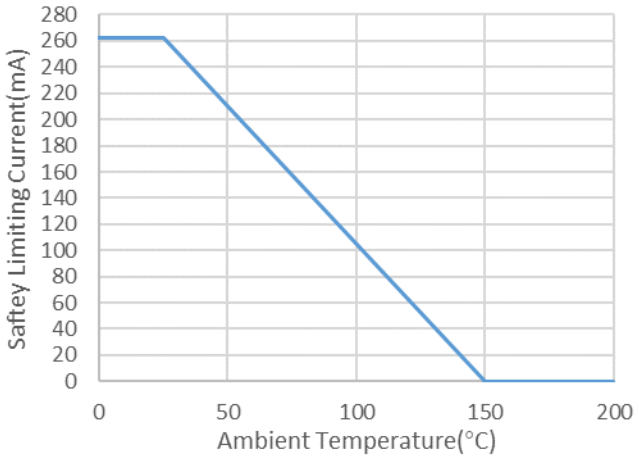

Figure 6.3 NSi822xW-DSWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

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6.3. Regulatory Information

The NSi8220N/NSi8221N/NSi8222N are approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3750V_{rms} Isolation voltage	Single Protection, 3750V_{rms} Isolation voltage	Basic Insulation 565Vpeak, V_{IOSM}=5384Vpeak	Basic insulation at 400V_{rms} (565Vpeak)
File (pending)	File (pending)	File (pending)	File (pending)

The NSi8220W/NSi8221W/NSi8222W are approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforced Insulation 2121Vpeak, V_{IOSM}=6250Vpeak	Reinforced insulation at 1500V_{rms} (2121Vpeak)
File (pending)	File (pending)	File (pending)	File (pending)

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7. Function Description

7.1. Overview

The NSi822x is a Dual-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSi822x devices are high reliability dual-channel digital isolator with AEC-Q100 qualified. The NSi822x device is safety certified by UL1577 support several insulation withstand voltages (3.75kV$_{rms}$, 5kV$_{rms}$), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi822x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The NSi822x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi822x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSi822x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 4.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 60us after powering up.

Table 7.1 Output status vs. power status

Input	*VDD1 status*	*VDD2 status*	*Output*	*Comment*
H[1]	Ready	Ready	H	Normal operation.
L[2]	Ready	Ready	L	
X[3]	Unready	Ready	L H	The output follows the same status with the input within 60us after input side VDD1 is powered on.
X	Ready	Unready	X	The output follows the same status with the input within 60us after output side VDD2 is powered on.
Note: H=Logic high; L=Logic low;X=Logic low or logic high				

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7.2. OOK Modulation

NSi822x is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 7.1, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

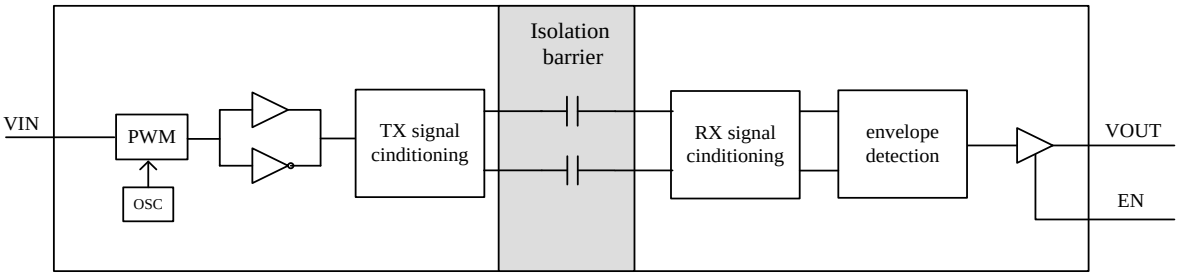

Figure 7.1 Single Channel Function Block Diagram

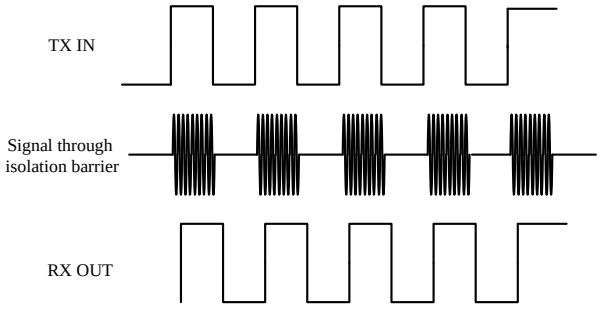

Figure 7.2 OOK Modulation

8. Application Note

8.1. Typical Application Circuit

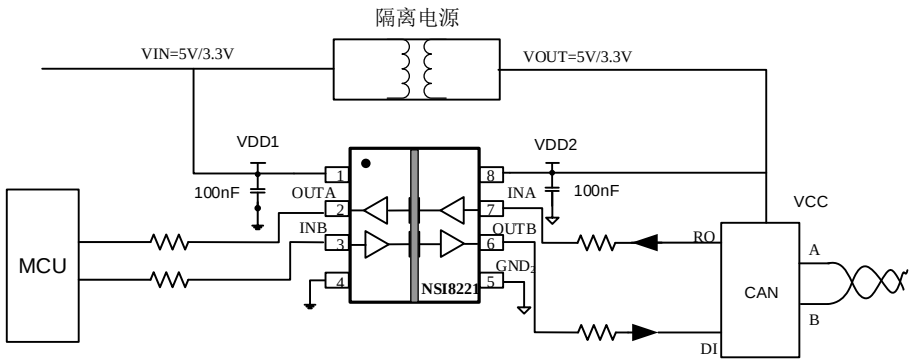

Figure 8.1 Typical SCH for ISO CAN Interface

8.2. PCB Layout

The NSi822x requires a 0.1 µF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be

placed as close as possible to the package. Figure 5.1 to Figure 5.4 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω, ±40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

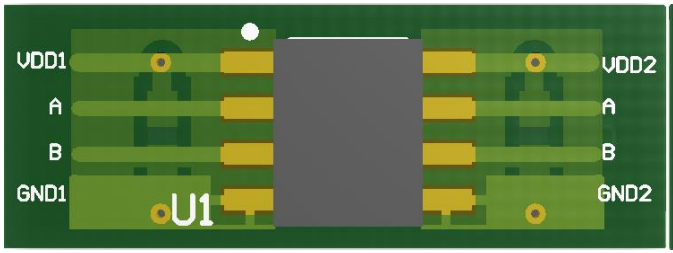

Figure8.1 Recommended PCB Layout — Top Layer

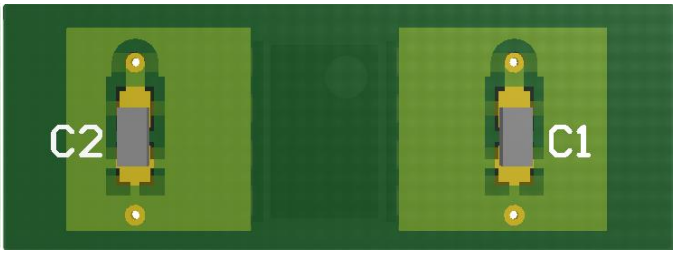

Figure8.2 Recommended PCB Layout — Bottom Layer

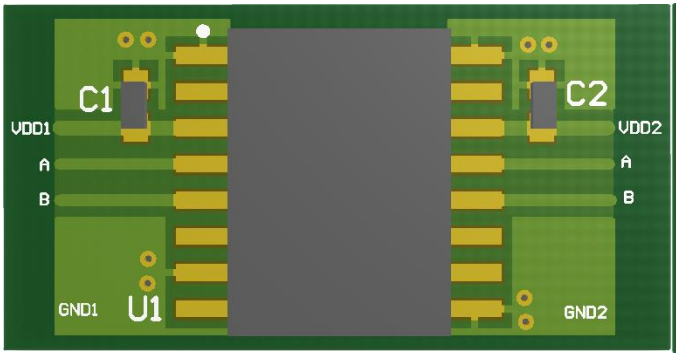

Figure8.3 Recommended PCB Layout — Top Layer

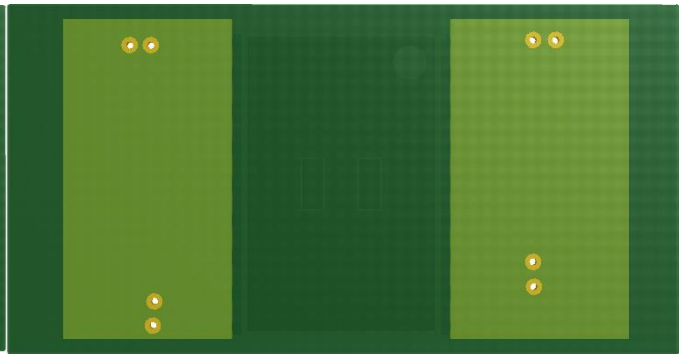

Figure8.4 Recommended PCB Layout — Bottom Layer

8.3. High Speed Performance

Figure 5.5 shows the eye diagram of NSi822x at 200Mbps data rate output. The result shows a typical measurement on the NSi822x with 350ps p-p jitter.

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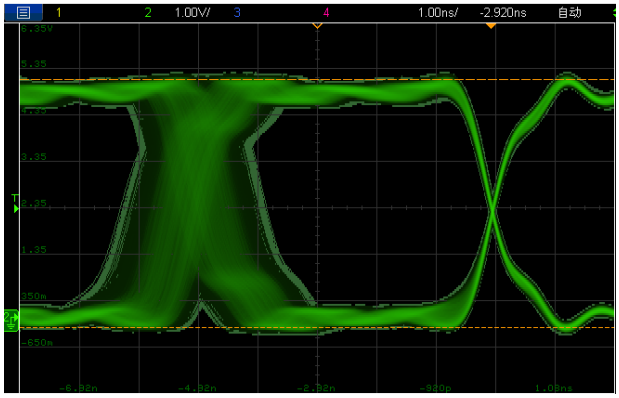

Figure8.5 NSi822x Eye Diagram

8.4. Typical Supply Current Equations

The typical supply current of NSi822x can be calculated using below equations. I_{DD1} and I_{DD2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF

NSi8220:

I_{DD1} = 0.19 *a1+1.45*b1+0.82*c1.

I_{DD2} = 1.36+ VDD1*f* C_L *c1*10^{-9}

When a1 is the channel number of low input at side 1, b1 is the channel number of high input at side 1, c1 is the channel number of switch signal input at side 1.

NSi8221/ NSi8222:

I_{DD1} = 0.87 +1.26*b1+0.63*c1+ VDD1*f* C_L *c2*10^{-9}

I_{DD2} = 0.87 +1.26*b2+0.63*c2+ VDD1*f* C_L *c1*10^{-9}

When b1 is the channel number of high input at side 1, c1 is the channel number of switch signal input at side 1, b2 is the channel number of high input at side 2, c2 is the channel number of switch signal input at side 2.

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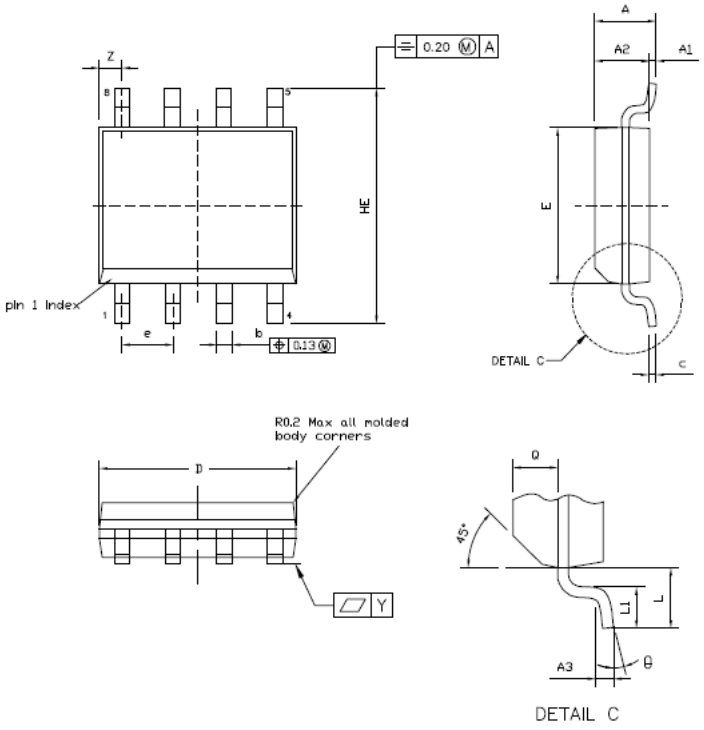
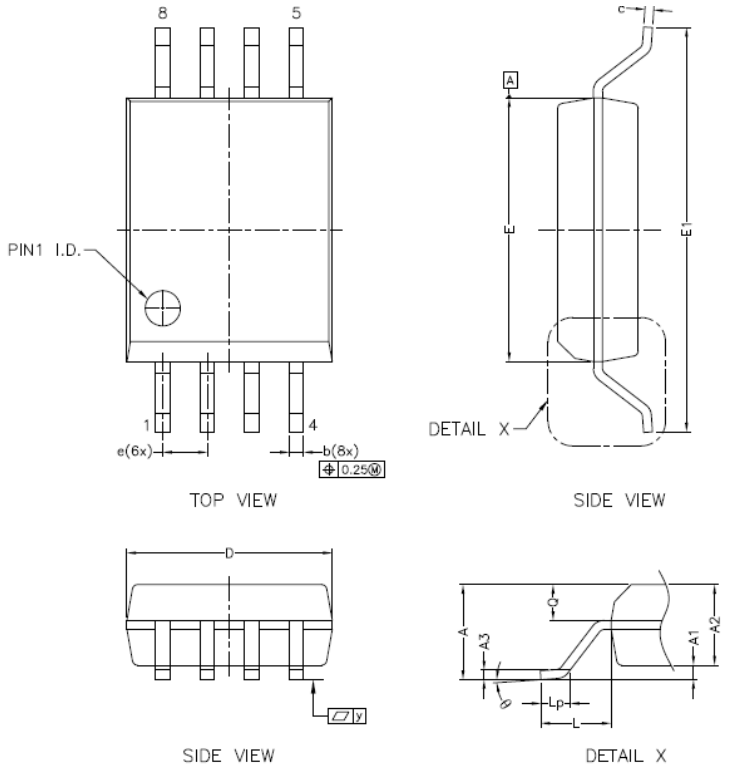
9. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.75
A1	0.10	---	0.25
A2	1.25	1.35	1.45
b	0.33	0.38	0.49
c	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
Q	0.60	0.65	0.70
HE	5.80	6.00	6.20
e	1.27 BSC		
L	1.05 BSC		
L1	0.40	0.64	1.00
Y	---	0.10	---
Z	0.3	0.5	0.7
A3	0.25 BSC		
θ	0°	5°	8°

Figure 9.1 SOP8 Package Shape and Dimension in millimeters (inches)



* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	--	--	2.80
A1	0.36	--	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	--	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	--	1.00
y	--	0.10	--
θ	0°	--	8°

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 9.2 SOW8 Package Shape and Dimension in millimeters and (inches)

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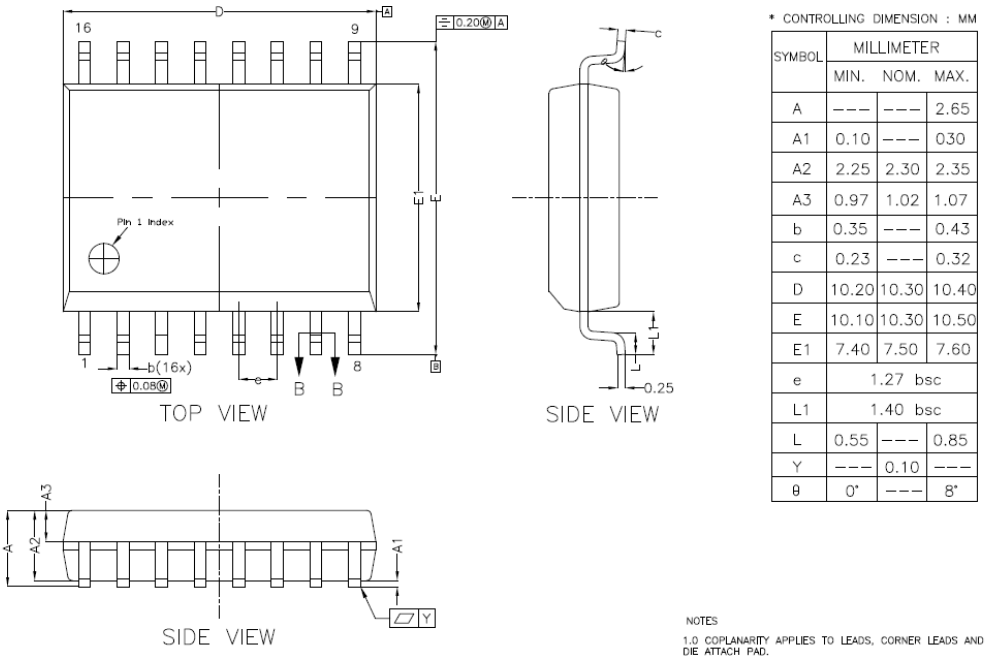

* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	030
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 9.2 SOW16 Package Shape and Dimension in millimeters and (inches)

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10. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSi8220N0-DSPR	3.75	2	0	150	Low	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8220N1-DSPR	3.75	2	0	150	High	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8221N0-DSPR	3.75	1	1	150	Low	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8221N1-DSPR	3.75	1	1	150	High	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8222N0-DSPR	3.75	1	1	150	Low	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8222N1-DSPR	3.75	1	1	150	High	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8220W0-DSWR	5	2	0	150	Low	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NSi8220W1-DSWR	5	2	0	150	High	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NSi8221W0-DSWR	5	1	1	150	Low	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NSi8221W1-DSWR	5	1	1	150	High	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NSi8222W0-DSWR	5	1	1	150	Low	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NSi8222W1-DSWR	5	1	1	150	High	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NSi8220W0-DSWVR	5	2	0	150	Low	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSi8220W1-DSWVR	5	2	0	150	High	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSi8221W0-DSWVR	5	1	1	150	Low	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSi8221W1-DSWVR	5	1	1	150	High	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSi8222W0-DSWVR	5	1	1	150	Low	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSi8222W1-DSWVR	5	1	1	150	High	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSi8220W0-Q1SWR	5	2	0	150	Low	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NSi8220W1-Q1SWR	5	2	0	150	High	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NSi8221W0-Q1SWR	5	1	1	150	Low	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NSi8221W1-Q1SWR	5	1	1	150	High	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NSi8222W0-Q1SWR	5	1	1	150	Low	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NSi8222W1-Q1SWR	5	1	1	150	High	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NSi8220W0-	5	2	0	150	Low	-40 to 125℃	3	SOW8	SOW8	1000

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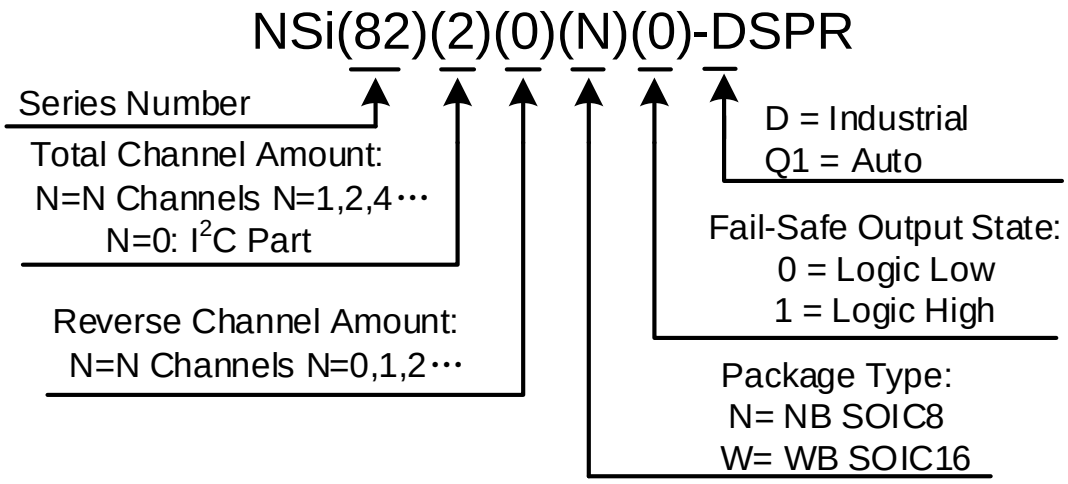
Q1SWVR								(300mil)		
NSi8220W1-Q1SWVR	5	2	0	150	High	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSi8221W0-Q1SWVR	5	1	1	150	Low	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSi8221W1-Q1SWVR	5	1	1	150	High	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSi8222W0-Q1SWVR	5	1	1	150	Low	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSi8222W1-Q1SWVR	5	1	1	150	High	-40 to 125℃	3	SOW8 (300mil)	SOW8	1000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures. All devices are AEC-Q100 qualified.										

Part Number Rule:



11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSI822x	Click here	Click here	Click here	Click here

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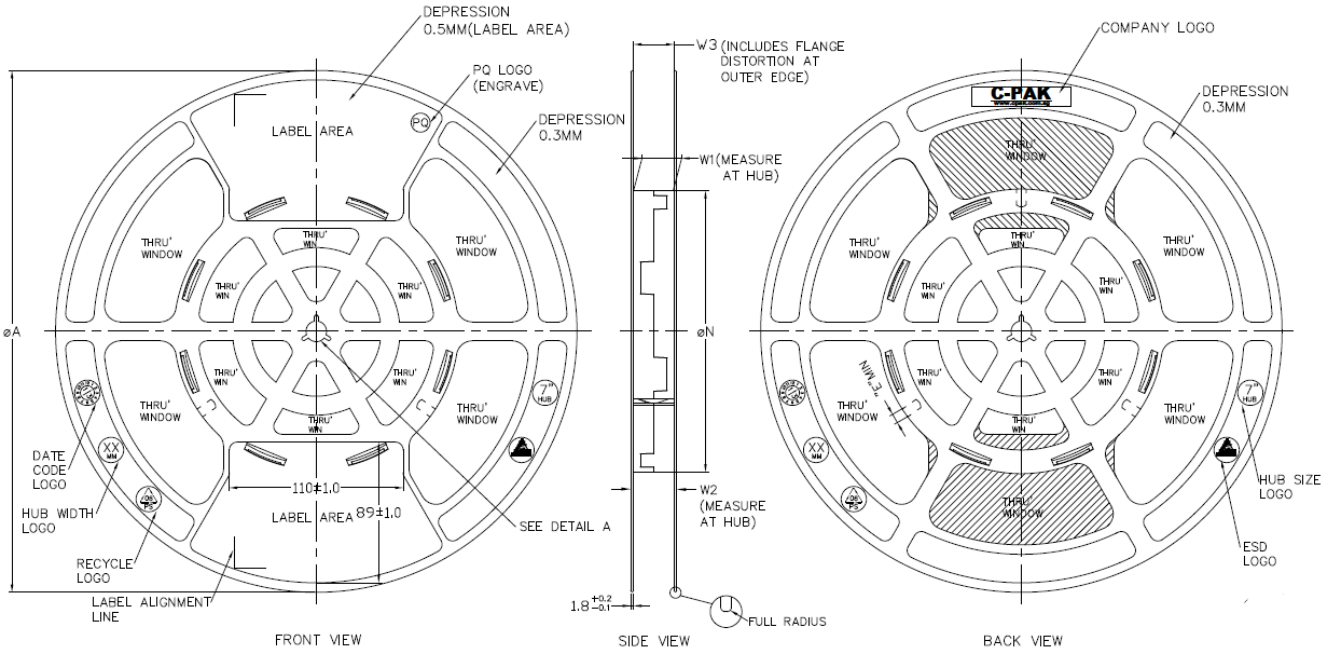
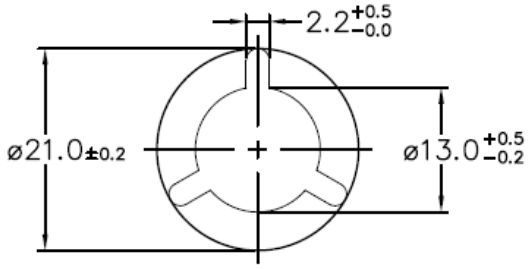
12. TAPE AND REELINFORMATION





ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

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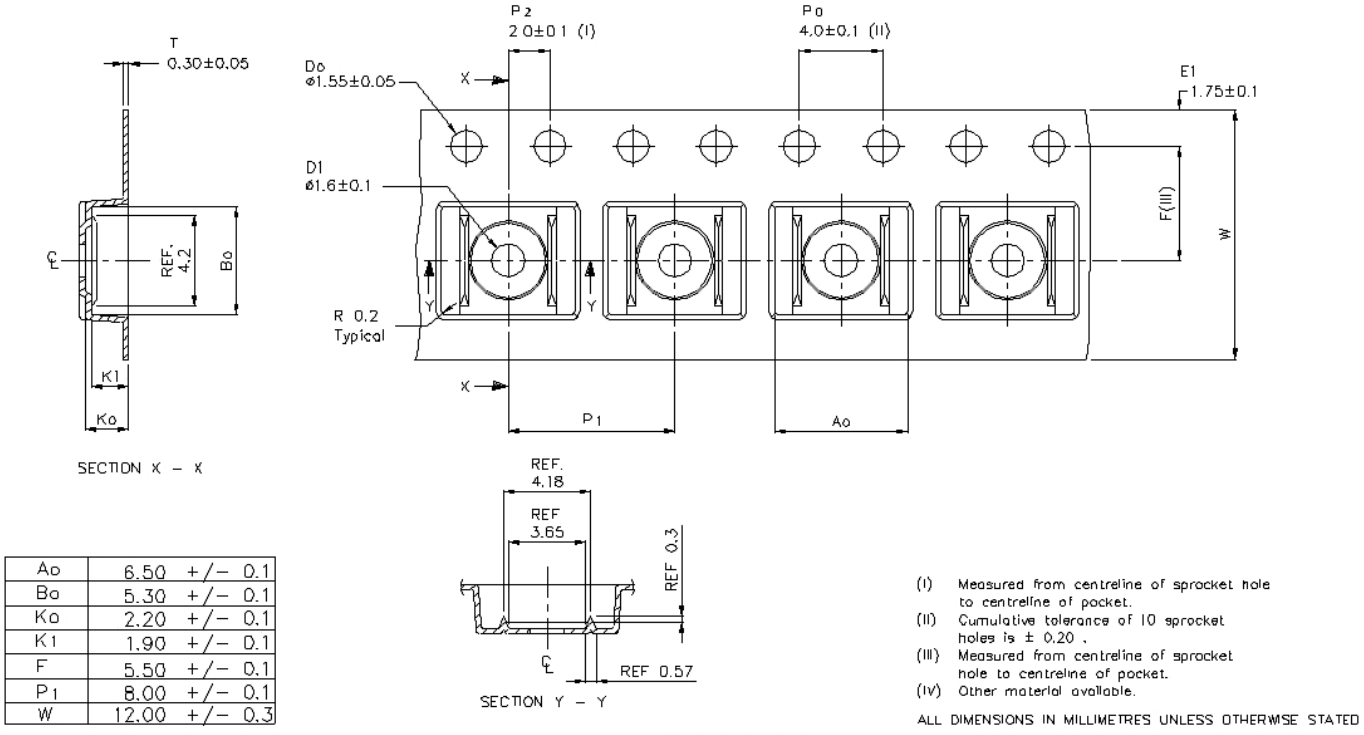
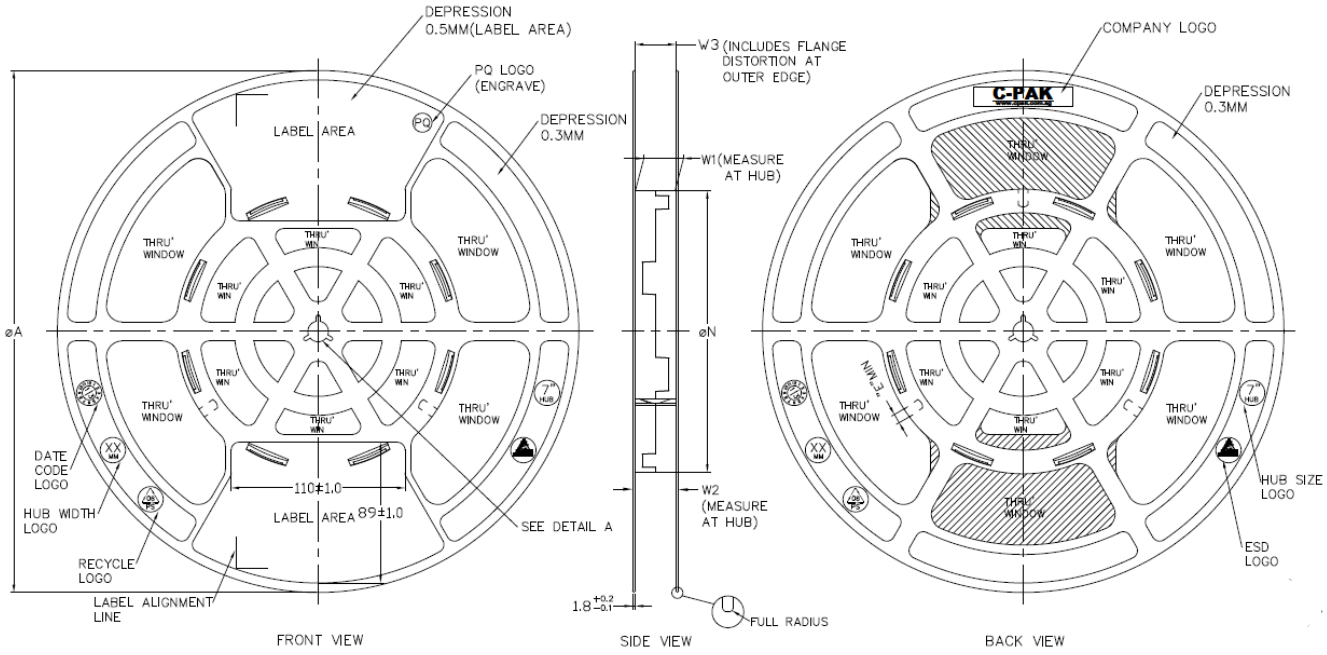
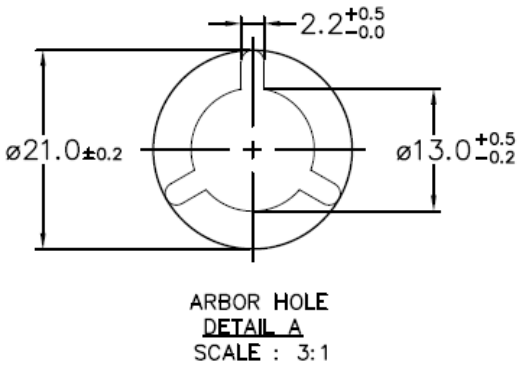


Ao	6.50	+/–	0.1
Bo	5.30	+/–	0.1
Ko	2.20	+/–	0.1
K1	1.90	+/–	0.1
F	5.50	+/–	0.1
P1	8.00	+/–	0.1
W	12.00	+/–	0.3

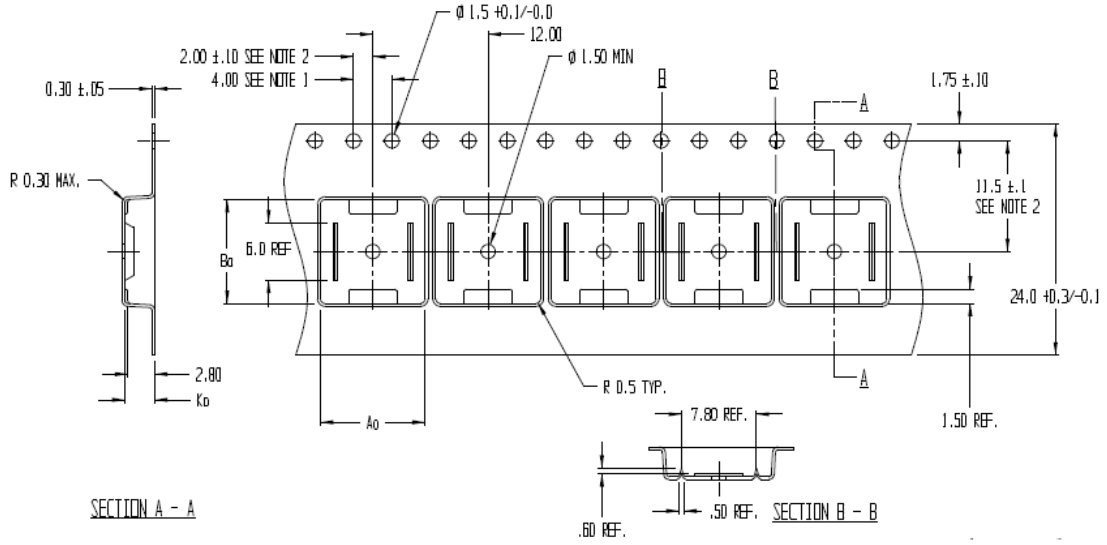
Figure 12.1 Tape and Reel Information of SOP8





PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
3. Ao AND Bo ARE CALCULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Ao = 10.90
Bo = 10.80
Ko = 3.1

Figure 12.2 Tape and Reel Information of WB SOW16

13. Revision History

Revision	Description	Date
1.0	Initial version	2019/12/20
1.1	Update SOW8 package PIN description	2020/6/23

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