General Clock Generator

PRODUCT DESCRIPTION

MS5351M is an I^{2}C configurable, 3-channel output clock generator chip, which can completely replace crystals, crystal oscillators, phase-locked loops, and output buffers used in cost-sensitive applications. Thanks to the use of fractional frequency phase locked loop and high-precision fractional frequency divider structure, MS5351M can generate any clock output from 2.5kHz to 200MHz.

FEATURES

- Highly integrated analog circuit to demodulate and decode
- 3 channels output non-integer related clocks from 2.5kHz to 200MHz
- I^{2}C user-defined configuration output clock
- Accurate frequency synthesis
- Low output jitter
- Can work with low-cost, fixed-frequency quartz crystals: 25MHz or 27MHz
- Output clock supports static phase shift
- Programmable control of output clock rise/fall time
- Glitch-free frequency switching
- Independent power supply pins Internal core circuit power supply VDD: 2.5V or 3.3V Output stage
- High internal power supply rejection ratio can save external filter capacitor
- Adjustable output delay
- Compatible with HCSL and PCIE Gen 1 applications

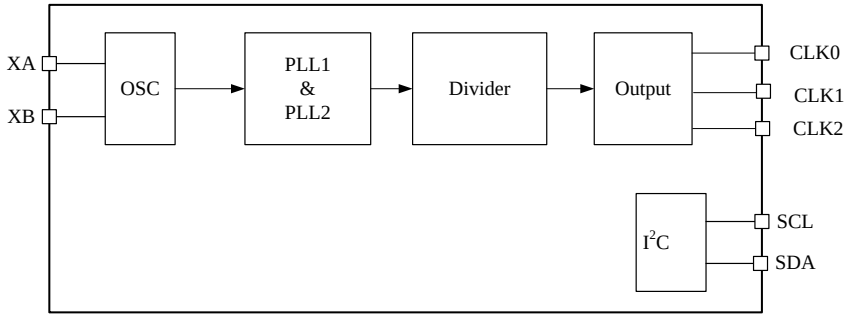
APPLICATIONS

- HD TV, DVD/Blu-ray, set-top box
- Audio/video equipment, Game consoles
- Printers, scanners, projectors
- Hand-held devices
- Home gateway equipment
- Network/communication
- Servers, storage
- Quartz crystal/crystal oscillator/phase-locked loop replacement

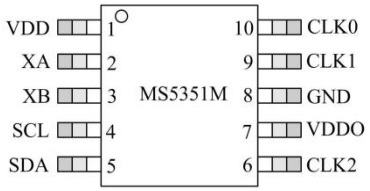
PACKAGE/ORDERING INFORMATION

Part Number	Package	Marking
MS5351M	MSOP10	MS5351M

SIMPLIFIED BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin	Symbol	Type	Description
1	VDD	power	Internal circuit power supply
2	XA	input	External quartz crystal input
3	XB	input	External quartz crystal input
4	SCL	input	I^2C clock input, at least 1kΩ pull-up resistor must be connected
5	SDA	input/output	I^2C data input/output, at least 1kΩ pull-up resistor must be connected
6	CLK2	output	Output clock
7	VDDO	power	Output stage power supply
8	GND	ground	Reference GND
9	CLK1	output	Output clock
10	CLK0	output	Output clock

ABSOLUTE MAXIMUM RATINGS

Note: It is not allowed to exceed the range of rated value in actual application.[1]

Table 1. Limiting Condition.

Parameter	Symbol	Condition	Rated value	Unit
Internal supply voltage	VDD		-0.5 to 3.8	V
Output stage supply voltage	VDDO		-0.5 to 3.8	V
Input pin voltage	VIN_SCL	SCL,SDA	-0.5 to 3.8	V
	VIN_XA/XB	XA,XB	-0.5 to 1.3	V
Junction temperature	T_J		-55 to 150	^oC
Soldering iron temperature (lead-free) [2]	T_{PEAK}		260	^oC
Duration of soldering iron temperature at T_{PEAK} (lead-free) [2]	T_P		10	Second

[1] Exceeding the absolute rated maximum value may cause permanent damage to the chip

[2] The chip meets the JEDEC J-STD-020 specification

RECOMMEND OPERATING CONDITION

Table 2.Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
Operating temperature	T_A	-40	25	105	°C
Internal circuit voltage	VDD	3.0	3.3	3.6	V
		2.25	2.5	2.75	V
Output stage voltage	VDDO	1.71	1.8	1.89	V
		2.25	2.5	2.75	V
		3.0	3.3	3.6	V

ELECTRICAL CHARACTERISTICS

Table 3. Electrical characteristics (VCC=3.3V, TA = 25℃, unless otherwise noted.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DC Characteristic						
VDD Current	I_{DD}	3 channel output		33		mA
Single channel output stage current	I_{DDOx}	C_L=5pF, Less than 100MHz Maximum drive capacity		5		mA
Input Current	I_{SCL}	SCL,SDA			10	uA
Output impedance	Z_O	3.3V VDDO,High drive		50		Ω
AC Characteristic						
Power-on time	T_{RDY}	From VDDmin to effective output clock, f_{CLKn}>1MHz		2	10	ms
Power-on time when PLL bypass	T_{BYP}	From VDDmin to effective output clock, f_{CLKn}>1MHz		0.5	1	ms
Output frequency switching time	T_{FREQ}	f_{CLKn}>1MHz			20	us
Output phase shift	P_{STEP}			333		ps/step
Spread spectrum range	SS_{DEV}	Down spread spectrum, 0.1% per step	-0.1		-2.5	%
		Center spread spectrum, 0.1% per step	±0.1		±2.5	%
Spread spectrum modulation rate	SS_{MOD}		30	31.5	33	kHz
Crystal specifications						
Quartz crystal frequency	f_{XTAL}		25		27	MHz
Load capacitance	C_{XL}		6		12	pF
Equivalent series resistance	r_{ESR}				150	Ω
Maximum drive level	d_L		100			uW
Input voltage	$V_{IN\_XA/AB}$	XA and XB	-0.3		1.1	V
Output clock specification						
Output frequency	F_{CLK}		0.0025		200	MHz
Load capacitance	C_L				15	pF
Duty cycle	DC	F_{CLK}<160MHz	45	50	55	%
		F_{CLK}<160MHz	40	50	60	%
Rise Time	t_r	20%~80%,C_L=5pFMaximum drive		0.5	1.2	ns
Fall time	t_f	20%~80%,C_L=5pFMaximum drive		0.5	1.2	ns
Output high level	V_{OH}	C_L=5pF	VDD-0.6			V

Output low level	V_{OL}	C_L=5pF			0.6	V
Period jitter	J_{PER}	3 channels simultaneously output		60	180	ps,pk
Adjacent clock jitter	J_{CC}	3 channels simultaneously output		60	180	ps,pk

I^2C Specification（SCL, SDA）

Parameter	Symbol	Condition	Standard mode 100kbps		Fast mode 400kbps		Unit
			Min.	Max.	Min.	Max.	V
Low-level input voltage	V_{ILI2C}		-0.5	$0.3*V_{DDI2C}$	-0.5	$0.3*V_{DDI2C}$	V
High-level input voltage	V_{IHI2C}		$0.7*V_{DDI2C}$	3.6	$0.7*V_{DDI2C}$	3.6	V
Schmidt hysteresis voltage	V_{HYS}		-	-	0.1	-	V
Low-level output voltage	V_{OLI2C}	V_{OLI2C}=2.5/3.3V, Open drain, 3mA current sink	0	0.4	0	0.4	V
Input Current	I_{II2C}		-10	10	-10	10	uA
Pin capacitance	C_{I2C}	VIN=-0.1toV_{DDI2C}	-	4	-	4	pF
I^2CBus pause time	T_{TO}	Pause enable	25	35	25	35	ms

NOTE:

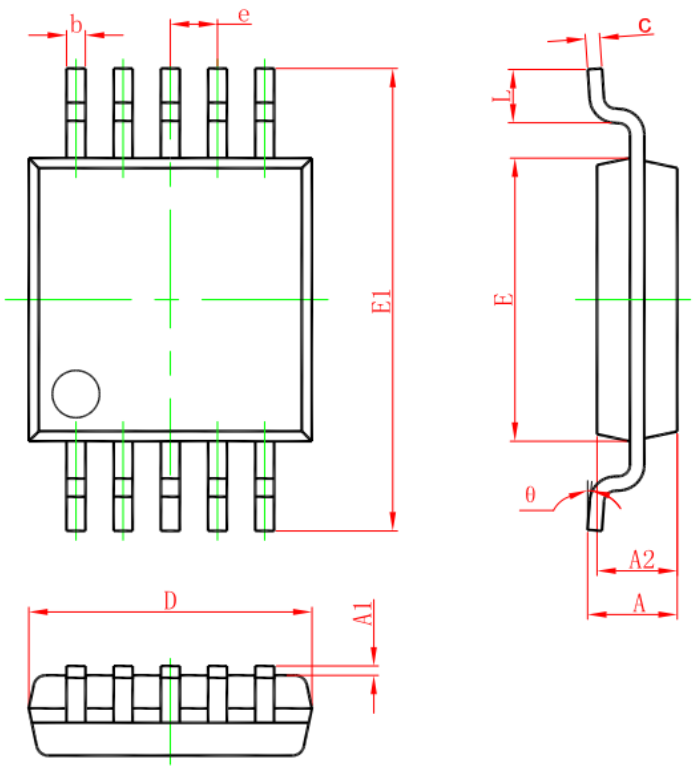
[1] Only 2 clocks larger than 112.5MHz are allowed to be output at the same time

[2] The clock jitter test is 10000 cycles, and measured at the maximum output drive capacity

[3] Jitter is highly dependent on frequency configuration

[4] I^2C only supports 2.25V to 3.6V power supply

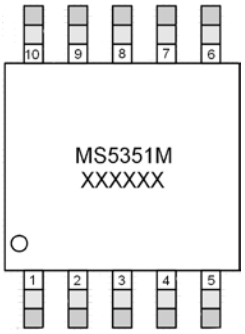
PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.50(BSC)		0.020(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

Marking and Packaging Specifications

1. Marking drawing description



MS5351M：Product name

XXXXXX：Product code

2. Marking drawing pattern

Laser printing， contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	piece/reel	reel/box	piece /box	box/carton	piece/carton
MS5351M	MSOP10	3000	1	3000	8	24000

REVISION HISTORY

Revision	Revision Date	Description	Page
V1.0	2021.03.08	First Version	10
V1.1	2021.06.30	Add 3.3V supply voltage for VDDO of Table2 on page 5	10

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don’t release additional notice.
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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS circuit operation precautions:

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must be used conductor packaging or antistatic materials packaging or transportation.

+86-571-89966911

Room 701， No.9 Building,No.1, WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

http:// www.relmon.com