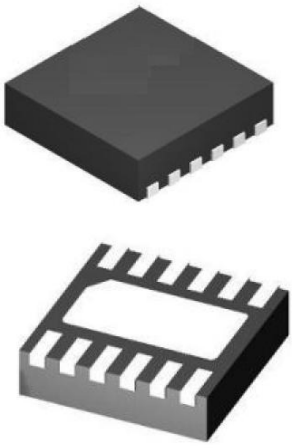
24bit, 192kHz Dual Channel Differential Digital to Analog Converter

PRODUCT DESCRIPTION

The MS5281D is a stereo digital-to-analog converter chip, which contains interpolation filter, a multi-bit Δ-Σ modulator, differential output analog filter. The MS5281D supports most of audio data formats. It is based on the fourth order of a linear analog low pass filter and multi-bit Δ-Σ modulator. The MS5281D can automatically adjust the sample rate from 2kHz and 200kHz by detecting signal frequency and master clock frequency.

The MS5281D can operate at 3.3V and 5V. These features make it ideal for wireless devices such as DVD playback decoders and digital communication devices. The MS5281D is available in DFN12 package.



DFN12

FEATURES

- Muti-bit ΔΣ Modulator
- 24bit D/A Converter
- Automatic Detection of Signal Frequencies up to 192kHz
- DR: 110dB
- THD: 0.003%
- Low Clock Jitter Sensitivity
- 3.3V or 5V Operating Voltage
- Linear Filter Output
- DFN12 Package

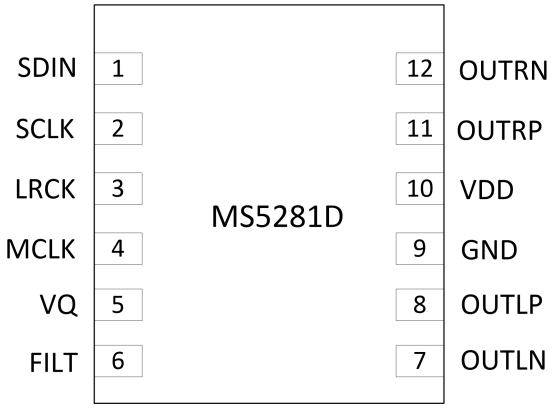
APPLICATIONS

- Digital Communication Equipment
- Car Audio System
- DVD Audio System

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS5281D	DFN12	5281D

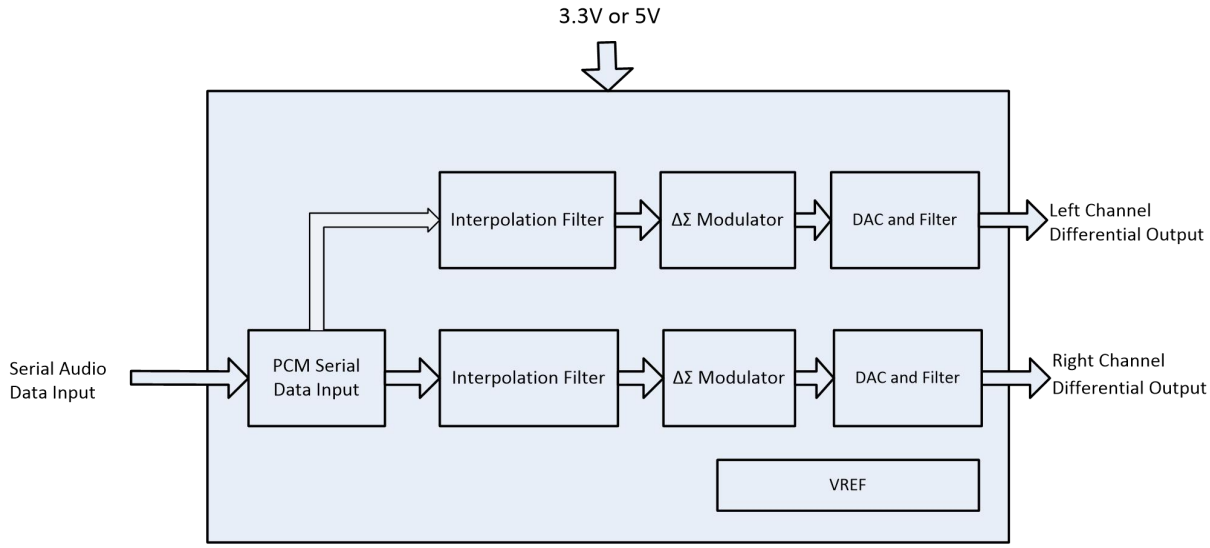
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	SDIN	I	Serial Audio Data Input
2	SCLK	I	External Serial Clock Input
3	LRCK	I	Left or Right Clock
4	MCLK	I	Master Clock
5	VQ	IO	DC Voltage
6	FILT	IO	Positive Reference Voltage
7	OUTLN	O	Left Channel Negative Analog Output
8	OUTLP	O	Left Channel Positive Analog Output
9	GND	-	Ground
10	VDD	-	Power
11	OUTRP	O	Right Channel Positive Analog Output
12	OUTRN	O	Right Channel Negative Analog Output

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	VDD	-0.3~ 7	V
Input Current	I_{in}	-10 ~ +10	uA
Digital Input Voltage	V_{IND}	-0.3 ~ VDD+0.3	V
Operating Temperature	T_{OP}	-55 ~ 125	°C
Storage Temperature	T_{stg}	-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Range			Unit
		Min	Tyo	Max	
Power Supply	VDD	3.0		5.5	V
Temperature Range	T_A	-40		+85	°C

ELECTRICAL CHARACTERISTICS

DAC Analog Characteristics

TA = 25°C, Full-scale Output Sinusoidal Signal, 997Hz, Fs = 48/96/192kHz;
RL=3kΩ, CL=10pF, Test Bandwidth 10Hz to 20kHz.

Parameter			3.3V			Unit
			Min	Typ	Max	
DR	24 bit	A-weighted	100	102		dB
THD	24 bit	0dB	0.003			%
		-60dB	0.1	0.3		%
Isolation						
Inter Channel Isolation (1kHz)			95	100		dB
DAC Accuracy						
Inter Channel Gain Mismatch				0.1	0.2	dB
Analog Output						
Full Scale Output Voltage			0.63×VDD	0.66×VDD	0.69×VDD	Vpp
DC Voltage (V_Q)				0.5×VDD		VDC
Maximum DC Current at AOUT pin (I_{OUTmax})				3.3		mA
Maximum Current at VQ pin (I_{Qmax})				1		mA
Maximum AC-Load Resistance (R_L)				1		kΩ
Maximum Load Capacitance (C_L)				1000		pF
Output Impedance (Z_{OUT})				110		Ω

Filter Characteristics

Parameter		Min	Typ	Max	Unit
Single-Speed Mode					
PassBand	to -0.1dB Corner			0.35	Fs
	to -3dB Corner			0.4992	Fs
Frequency Response from 40Hz to 15kHz		-0.07		+0.55	dB
StopBand		0.54			Fs
StopBand Attenuation		55			dB
Group Delay(Tgd)			10/fs		s
Double-Speed Mode					
PassBand	to -0.1dB Corner	0		0.22	Fs
	to -3dB Corner	0		0.501	Fs
Frequency Response from 40Hz to 15kHz		-0.02		+0.2	dB

Parameter		Min	Typ	Max	Unit
StopBand		0.54			Fs
StopBand Attenuation		55			dB
Group Delay(Tgd)			5/Fs		s
Quad-Speed Mode					
PassBand	to -0.1dB Corner	0		0.11	Fs
	to -3 dB Corner	0		0.469	Fs
Frequency Response from 40Hz to 15kHz		-0.01		+0.1	dB
StopBand		0.54			Fs
StopBand Attenuation		55			dB
Group Delay(Tgd)			2.5/Fs		s

Digital Input Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}	VDD-0.6			V
Low-Level Input Voltage	V_{IL}			0.6	V
Input Leakage Current	I_{in}		0.02		uA
Input Capacitance			3	8	pF

Power Characteristics

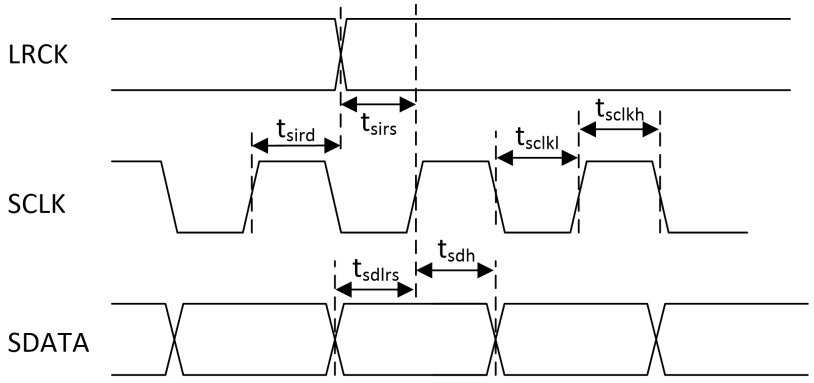
Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current	Normal Operation(3.3V)	I_A		16	25	mA
	Power Down state(3.3V)	I_A		100		uA
Power Supply Rejection Ratio	1kHz(3.3V)	PSRR		70		dB
	60Hz(3.3V)			50		dB

Switching Characteristics (Serial Interface)

Parameter		Symbol	Min	Typ	Max	Unit
MCLK Frequency			2		50	MHz
MCLK Duty Cycle			45		55	%
Input Sample Rate (MCLK/LRCK)	256x,384x,1024x	Fs	8		50	kHz
	256x,384x		84		134	kHz
	512x,768x		42		67	kHz
	1152x		30		34	kHz
	128x,192x		50		100	kHz
	64x,96x		100		200	kHz
	128x,192x		168		200	kHz

Parameter	Symbol	Min	Typ	Max	Unit
LRCK Duty Cycle (External SCLK only)		45	50	55	%
SCLK Pulse Width Low	tsclkl	20			ns
SCLK Pulse Width High	tsclkh	20			ns
SCLK Duty Cycle		45	50	55	%
SCLK Rising to LRCK Edge Delay	tslrd	20			ns
SCLK Rising to LRCK Edge Setup Time	tslrs	20			ns
SDIN Valid to SCLK Rising Edge Setup Time	tsdlrs	20			ns
SCLK Rising to SDIN Hold Time	tsdh	20			ns

External Serial Interface Input Timing



FUNCTIONAL DESCRIPTION

The MS5281D accepts standard audio sampling frequency, including 48, 44.1, 32kHz in QSM mode, 96 , 88.2 and 64kHz in DSM mode, 192, 176.4, 128kHz in SSM mode. Audio data is entered through serial input data terminal (SDIN). LRCK determines the channel of the present input data. A serial clock is a clock where audio data enters the input data cache.

Master Clock

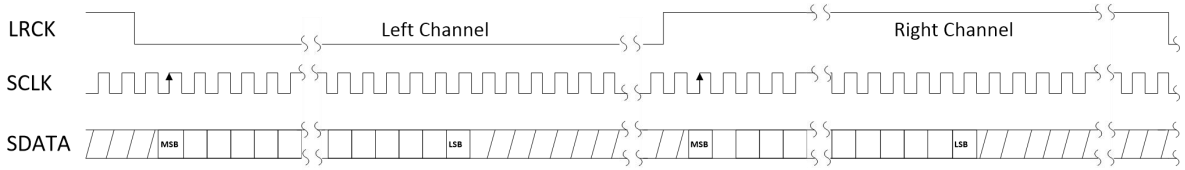
The MCLK/LRCK ratio must be an integer, as shown in table 1 below. The frequency of LRCK is equal to the frequency Fs of input data for each channel. The ratio of MCLK to LRCK and the speed mode are initialized by calculating the number of MCLK cycles and the value of MCLK within an LRCK period. A built-in divider will produce a proper clock. The following table lists some of the audio sampling frequencies, along with the corresponding MCLK and LRCK frequencies. Note that although there is no phase requirement, the LRCK and MCLK must be synchronized.

Table 1. Clock Frequencies

Mode	LRCK (kHz)	MCLK(MHz)					
		128x	256x	384x	512x	768x	1024x
QSM	32	-	8.192	12.288	16.384	24.576	32.768
	44.1	5.6448	11.2896	16.9344	22.5792	33.868	45.158
	48	6.144	12.288	18.432	24.576	36.864	49.152
DSM	64	8.192	16.384	24.576	32.768	49.152	-
	88.2	11.2896	22.5792	33.868	45.1584	-	-
	96	12.288	24.576	36.864	49.152	-	-
SSM	128	24.576	32.768	49.152	-	-	-
	176.4	22.5792	45.1584	-	-	-	-
	192	24.576	49.152	-	-	-	-

Serial Input Clock

When 16 rising edge pulses are detected continuously at SCLK port during an LRCK cycle, an external serial input clock is entered.



I^2S, Up to 24-bit Data, Data valid on rising edge of SCLK

MS5281D Data Format (I^2S)

Initialization and Power Down

When the system is initially powered up, it enters the power-down state. At this time, the interpolation filter and Δ-Σ modulator are reset. The internal reference voltage, digital-to-analog converter, switched-capacitor filter, and low-pass filter are shut down until the system detects MCLK and LRCK clock. Once MCLK and LRCK are detected, the system starts to calculate the ratio of MCLK to LRCK, then powers up the internal reference voltage, and finally powers up the digital-to-analog converter, the switched-capacitor filter, and outputs the quiescent voltage VQ.

Output Transient Control

The MS5281D uses Pop-guard technology to reduce transient response during power-up and power-down.

Power Up

The DC level at the output terminal is provided by the VQ pin, which is low when the system is initially powered up. When MCLK detects this, VQ generates normal DC voltage. The start-up time is 400ms when a 10uF capacitor terminated to VQ pin.

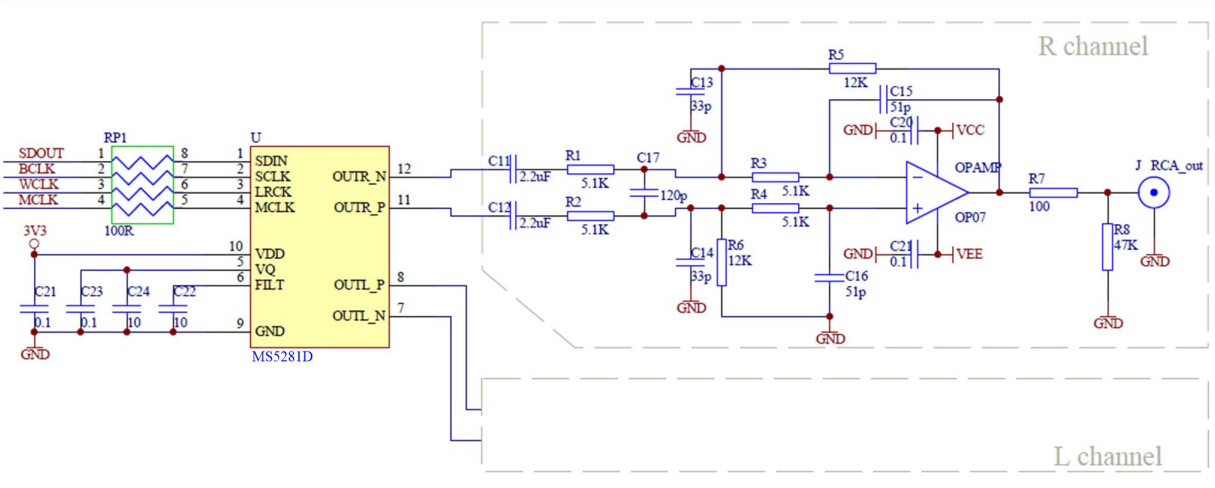
Power Down

To prevent transient pulses at the output terminal during power down, a 10uF capacitor is connected to the VQ pin. During this time, the VQ pin and the output pin gradually descend to GND. When it is necessary to change the clock frequency or sampling frequency, it is better to keep 10 cycles in the LRCK low level signal. The DAC keeps the low level output during the clock transformation.

Ground and Power Supply Decouple

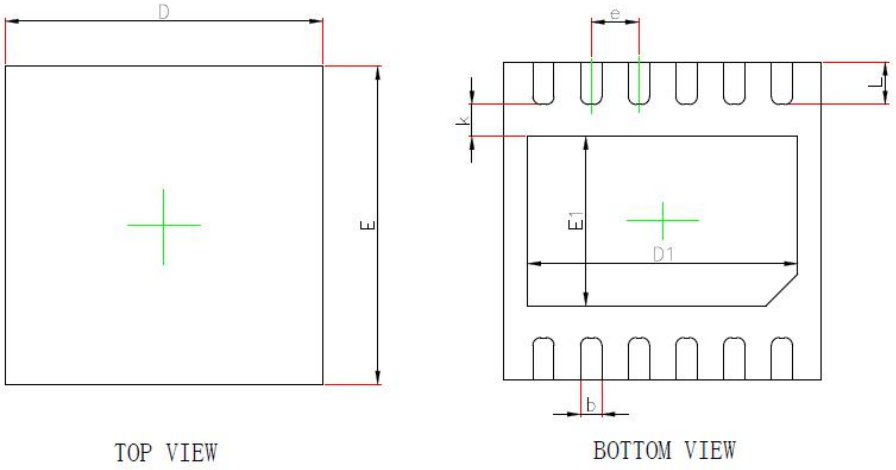
Be careful with ground and power connections to achieve desired performance. For best performance, the decoupling and filter capacitors must be placed as close as possible to the chip.

TYPICAL APPLICATION

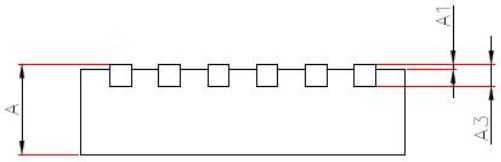


PACKAGE OUTLINE DIMENSIONS

DFNWB3X3-12L(P0.45T0.75/0.85)



TOP VIEW BOTTOM VIEW

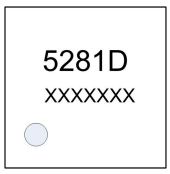


SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	2.450	2.650	0.096	0.104
E1	1.500	1.700	0.059	0.067
k	0.200MIN		0.008MIN	
b	0.150	0.250	0.006	0.010
e	0.450TYP		0.018TYP	
L	0.324	0.476	0.013	0.019

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name： 5281D

Product Code： XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Tray	Tray/Box	Piece/Box	Box/Carton	Piece/Carton
MS5281D	DFN12	5000	1	5000	8	40000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

  Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

+86-571-89966911

Rm701, No.9 Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

http:// www.relmon.com